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Tape bringt Fehler
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Honeywell

FIELD ENGINEERING

Series 16 4110/4120 MAGNETIC TAPE DRIVE OPTION MANUAL

42400343042

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H316 CP Instructions and Diagrams	70130072174	493
Instruction Manual Vols. 1, 2, 3		
DDP-416 General Purpose Computer	130071653/4/5	1035/6/7
DDP-516 General Purpose Computer	130071620/1/2	966/7/8
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SECTION 1
GENERAL DESCRIPTION

INTRODUCTION

The Honeywell Series 16-4110/4120 Magnetic Tape Option comprises up to four Magnetic Tape Transports (MTT's) and one 3 x 5 μ-BLOC Interface Control Module (TCU) with the associated interconnecting cables. The option number 4110 defines an installation comprising a single MTT with one TCU. The option includes Direct Memory Access (DMA) and Data Multiplexed Control (DMC) subchannel with automatic switching facilities as well as the standard I/O bus connection. To this option a further three MTT's, each supplied under option number 4120, can be added. Provision is made to allow the use of a second TCU with its' associated MTT's.

The information contained in this manual is concerned with the operation of the TCU. Details of the operation and maintenance of the device are contained in the Magnetic Tape Transport Manual Doc. No. 42400343041.

DATA CONTROL

The TCU contains all the logic circuitry necessary to handle control and data signals sent to it by the MTT's and the computer (CP). The TCU controls the following functions.

(a) Forward, Reverse and Rewind tape motion.

(b) Data transfer from tape to a 16-bit interface buffer.

(c) Data transfer from the buffer to the computer 'A'-register.

(d) Erase tape contents which are no longer required.

(e) Data transfer from the computer 'A'-register to a 16-bit interface buffer.

(f) Data transfer from the interface buffer to the tape.

(g) Write a file mark on tape.

(h) Move the tape forward or back one record or file.

(i) Utilise the DMA and DMC options.

POWER REQUIREMENTS

The TCU has a maximum static power requirement of Watts. The +6 volts power supply is obtained from the CP main frame supply circuits.

PHYSICAL CHARACTERISTICS

The TCU comprises a 3 x 5 μ-BLOC which may be located in the main frame tilt out cabinet if space permits, or in an I/O cabinet. Details of μ-PACs are given in the Instruction Manual for μ-PAC I/C modules Doc. No. 130071639. Other u-PACs are described in the Appendix to this manual.

PERFORMANCE SPECIFICATION

The 4120 Magnetic Tape Transport has the following performance specification:-

Operating Speed	16 inches per second
Start Time	4 milli-seconds to 5% of nominal speed
Stop Time	5 milli-seconds maximum
Rewind Time	10 minutes for full reel
Character Transfer Rate	High - 556 bits per inch (8.9 kHz) Low - 200 bits per inch (3.2 kHz)

TAPE SPECIFICATIONS

The MTT is designed to operate best when Honeywell Inc. or IBM certified 556/800 BPI heavy duty mylar tape with the following dimensions is used:-

Width	$\frac{1}{2}$ inch nominal
Thickness	1 - $1\frac{1}{2}$ mil
Reel Size	10.5 inches IBM compatible hub with file protect ring.

Honeywell certified magnetic tape; Honeywell specification number 05-390007-002 is recommended. Other tape of comparable quality may be used but the same degree of MTT performance is not guaranteed.

TAPE FORMAT

The data is written on tape using the 'Non Return to Zero Invert (NRZI) method. Each time a one bit is written on tape the write head current is inverted resulting in a polarity reversal on the tape. No polarity reversal results in a binary zero.

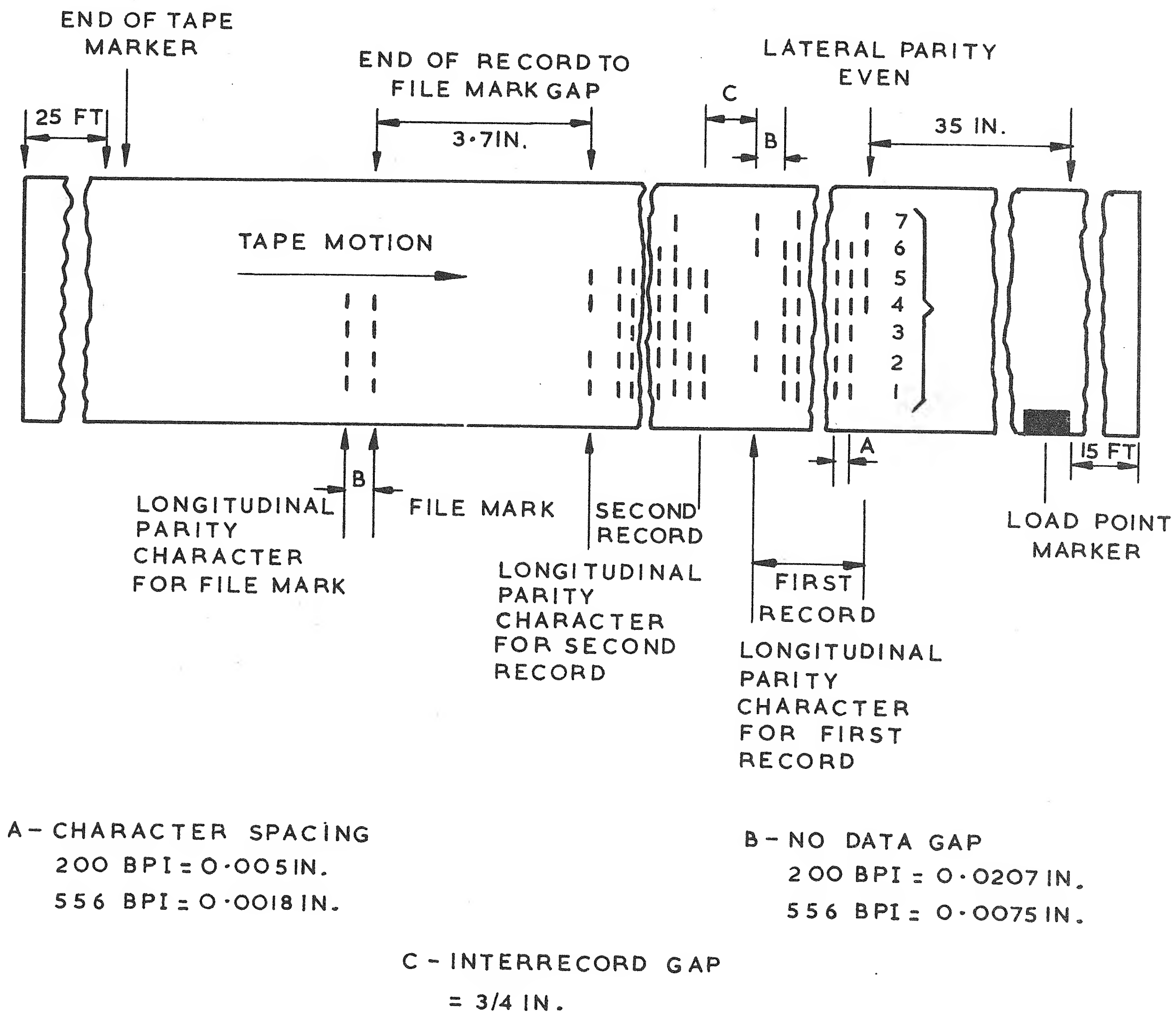


Figure 1-1 Magnetic Tape Format

Seven channels are contained along the tape and data is stored in lateral frames. Each frame contains a 6-bit character and a lateral parity bit which is written in track 7. The parity bit ensures that the number of one bits in each character is even in the BCD mode and odd in the binary mode. Data is stored at frame densities of 200 or 556 bits per inch to yield nominal data transfer rates of 3,200 or 8,896 characters per second respectively.

The data is stored on the tape in the form of records whose lengths are variable. The length of a record is determined by the number of characters programmed for storage on tape by a single write order. Each record contains a longitudinal parity character separated from the end of the record by four frame spaces. In both BCD and Binary modes this character ensures that an even number of one bits are written in each channel and that unrecorded areas at each end of the record are of the same polarity. Records are separated by interrecord gaps of 0.75 inches in which no data is stored. The gap is detected during read operations and by read after write logic during write operations and used to stop tape motion.

A file mark can be written on the tape to index a record or group of records. The file mark is an octal 17 and is separated from the last record by 3.7 inches. A longitudinal parity character is written after the file mark and is also an octal 17.

Reflective markers are attached at each end of the tape to mark the beginning and end of the usable portion of the tape. They are sensed by the MTT and the signals derived used to stop tape motion.

Data Word Construction

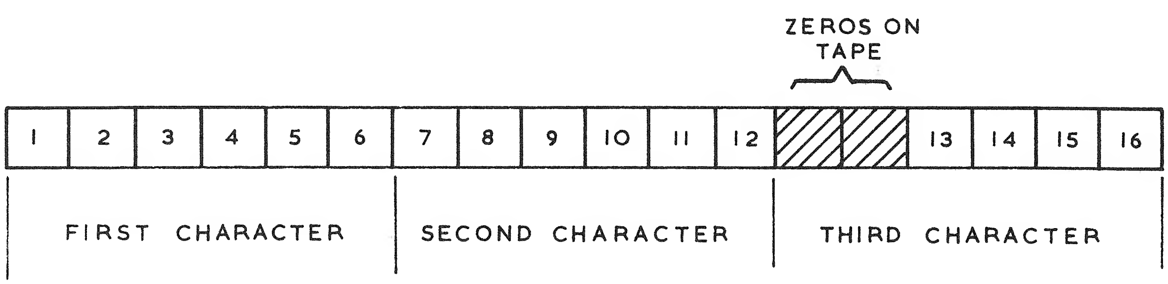


Figure 1-2 Character Per Word Construction

The character word construction is shown in Figure 1-2 which contains both two character per word and three character per word constructions. Computer words of 12-bits are contained in two consecutive frames in both BCD and binary modes. Three characters per word are used in the 16-bit binary mode in which case tracks 1 and 2 of the third character in each word are zeros and not used.

Code Compatibility

IBM code compatibility is achieved in the two characters per word mode only. Tape format and amplitudes are compatible with the IBM requirements for NRZI recordings and these tapes are compatible for use with IBM 729 series tape transports.

FUNCTIONAL DESCRIPTION

Reading

Selective commands from the CP to the TCU initiate motion control signals and the required MTT is set in motion. The erase head is disabled to prevent accidental erasure of tape contents. The tape passes under the read/write head at 16 inches per second and the data read character serially. The data is amplified to logic level by the logic contained in the MTT and strobed into the TCU word forming buffer. The lateral parity of each character is checked whilst word formation is taking place and if found incorrect a parity error signal is sent to the CP. Each character in the record is also entered into the longitudinal parity checker. The action of this checker is cumulative and counts the number of one bits written in each track of the tape. When the longitudinal parity character is read at the end of the record it is compared with the contents of the checker and if found incorrect a parity error signal is sent to the CP.

When a word is assembled in the word forming buffer a ready indicator is set to inform the CP that data is ready for transfer. The CP detects this ready state, initiates a data via the input bus (INB) and resets the word forming buffer and ready indicator.

The TCU detects the interrecord gap which follows the longitudinal parity character and generates motion reset signals to halt tape motion. If the CP issues a further command which requires continuation of tape motion in the same direction however, the motion continues uninterrupted.

Writing

The selected MTT is set in motion as when reading but with the erase head enabled. The TCU informs the CP that it is ready to receive data and a complete word is applied to the buffer via the output bus (OTB). The ready indicator is reset and the high or low density clock as selected by the density select switch on the MTT is enabled to generate the frame rate. The first character (bits 01 through 06) is transferred to the NRZ register and a lateral parity bit generated. A write pulse is generated by the TCU and the first character transferred to the MTT for writing on tape.

With bits 01 through 06 on tape the word bits 07 through 12 are processed in similar manner. With the three-character-per-word mode selected the buffer character distribution is set to transfer a third character.

Writing continues until the last word in the record is transferred from the CP. When this last word is written a longitudinal parity character is generated by the TCU

and written four frame spaces after the last data character. The end of record gap is detected by read after write network and used to generate motion reset signals which halt tape motion.

Write End of File

A file mark containing an octal 17 character can be written after a record. A write oscillator delay is initiated by the CP command and sustained for long enough to enable an end of record to file mark gap of 3.7 inches. The NRZ register is loaded with the file mark code which is then written on tape. A longitudinal parity character is written four frame spaces later and tape motion stopped as in normal write mode.

DMA/DMC SUBCHANNEL

The DMA and DMC subchannels permit the TCU to communicate with the CP by way of the DMA and DMC options. Provision is made for automatic subchannel switching for more efficient data handling with minimum program intervention.

MAINTENANCE

The maintenance section of the Central Processor Instruction Manual Vol. 1 contains general maintenance procedures for maintaining logic blocks. However apart from periodically checking the timing of monostables (as stated in the LBD's) no systematic scheme of maintenance is required.

A Verification and Test Program X16-MTT2 is provided to check for correct operation of the Magnetic Tape System. Full details of the use and operation of this program are contained in the X16-MTT2 program listing supplied.

Table 1-1 Option 4110 μ-PAC Complement

μ-PAC Model	Quantity	Type	Comprising
CC-088	5	Counter PAC	6 x flip-flops
CC-089	5*	Gated Flip-flop	4 x gated flip-flops
CC-092	10	Buffer Register	6 x flip-flops
CC-130	1	Resistor PAC	20 x 1K resistor loads
CC-138	1	Delay Multivibrator	2 x monostable
CC-139	1	Delay Multivibrator	2 x.monostable

Table 1-1 (Cont) Option 4110 μ-PAC Complement

μ-PAC Model	Quantity	Type	Comprising
CC-151	1	NAND Gate PAC	10 x 2-input NAND with separate load
CC-152	1	Transfer Gate PAC	14 x 2-input NAND with common inputs
CC-165	3*	Six Volt Line Driver	6 x clamp switches
CM-022	1*	Parallel Transfer Gate PAC	4 x NAND gate structures with common inputs
DC-335	2	Multi Input NAND	2 x 6-input NAND with mode 4 x 3-diode clusters
DI-335	11*	NAND Type 1	8 x 2-input NAND 2 x 2-input NAND with separate load
DL-335	5*	NAND Type 2	4 x 4-input NAND 2 x 4-input NAND with separate load
DM-335	2	Delay Multivibrator	2 x monostable
DN-335	2	Expandable NAND PAC	4 x 3-input NAND with modes 2 x 3-input NAND with modes and separate loads
EO-335	3	Exclusive OR PAC	5 x exclusive OR structures 1 x NAND
FF-335	2	Flip-Flop PAC	8 x flip-flops
NC-001	1	Delay Multivibrator	2 x monostable
NC-002	1	Delay Multivibrator	2 x monostable
NC-003	1	Delay Multivibrator	2 x monostable
NC-004	1	Delay Multivibrator	2 x monostable
NC-005	1	284.2 kHz Clock	1 x crystal controlled oscillator with pulse shaper
NC-006	1	204.2 kHz Clock	1 x crystal controlled oscillator with pulse shaper
OD-335	1	Octal Decimal Decoder	1 x octal matrix 2 x 6-input NAND with modes
PA-336	3	Power Amplifier	6 x 3-input power NAND with over current protection
TG-335	14	Transfer Gate PAC	4 x NAND gate structures with common input

* Denotes u-PAC complement for single MTT option only. Additional μ-PAC's are required for second, third and fourth MTT's and for DMC/DMA subchannel as follows:-

CC-089	-	One required for DMC/DMA subchannel
CC-165	-	Three required for each additional MTT
CM-022	-	Two required for each additional MTT
DI-335	-	Two required for each additional MTT
		Two required for DMC/DMA subchannel
DL-335	-	One required for DMC/DMA subchannel

The locations of these additional μ-PAC's are identified in the PAC allocation charts LBD No.'s E033 and E034.

SECTION 2
INSTALLATION

PHYSICAL DESCRIPTION

The TCU is connected to each MTT by two standard 32 conductor twisted pair cables. The cable assemblies are made to customers requirements for each installation within a maximum permissible length of 50 feet. The TCU ends of these cables are terminated with standard µ-PAC cable-PAC connectors and the MTT ends with Honeywell type 5JKVO-D67-06-3584 connectors.

Connection between the TCU and the CP is effected by use of standard jumper µ-PAC's. In the standard I/O mode all communication between the CP and TCU is by way of the I/O bus. In the DMA/DMC mode connections between TCU and CP are made via the DMA/DMC options.

EQUIPMENT DETAILS

The layout of the 3 x 5 µ-PAC TCU module is illustrated in LBD No.'s E033 and E034. Details of the cable assemblies connecting the TCU to the MTT's with signal mnemonics and connector pin assignments are shown in LBD No.'s E035 and E036. The signal mnemonics and connector pin assignments between the TCU and CP are given in LBD No. E032.

The standard parallel I/O bus comprises the following:-

(a) Ten address lines (twisted pair) ADB07 through ADB16, referred to as the address bus (ADB)

(b) Sixteen input lines (twisted pair) INB01 through INB16, referred to as the input bus (INB). When INB is quiescent the voltage level is +6 volts.

(c) Sixteen output lines (twisted pair) ITB01 through OTB16 referred to as the output bus (OTB).

(d) Control Lines:-

OCPLS	-	Carries an output control pulse during OCP commands to enable the command to be carried out.
SMKXX	-	Carries the set mask general output strobe.
SMK01	-	Carries an output control pulse to strobe the contents of the OTB into the mask flip-flop during an SMK instruction.

RRLIN	-	Carries a control pulse used to clear the TCU buffer and reset the ready indicator.
CMKXX	-	Carries a control pulse used to clear the set mask flip-flop.
DRLIN	-	Used to indicate to the CP the device status in reply to INA, OTA and SKS instructions.
PIL00	-	Carries an input control level used to request a program interrupt.
PARCK	-	Carries an input control level used to indicate a parity error.
ERLXX	-	Carries an input control pulse used by the DMC to indicate that memory end of range has been reached for the current DMC channel.
PWRFL	-	Carries an output control level used to warn the options that the CP is about to lose a.c. power.
MSTCL	-	Carries an output control level used to initialise all devices connected to it.

SECTION 3
PROGRAMMING INFORMATION

INSTRUCTION FORMAT

General information on programming is given in:-

(a) Doc. No. 42400343401 316/516 Programmers Reference Manual.

(b) Doc. No. 130071628 DDP-416 Programmers Reference Manual.

Programmed commands and instructions from the CP to the TCU are delivered via the I/O bus output and address lines. The instruction format is shown in Figure 3-1.

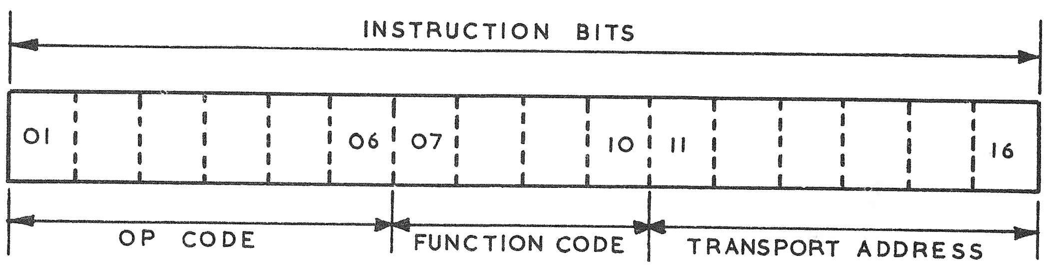


Figure 3-1 Instruction Format

The output code and function code are translated by the TCU logic into instructions for the tape transport. The TCU logic is shown in the logic block diagrams (LBD's) at the rear of this manual.

In any given system there may be one or two TCU's controlling up to eight MTT's. The standard address assignments, instruction bits 11 through 16 are as follows:-

TCU	MTTA	MTTB	MTTC	MTTD
No. 1	10_8	11_8	12_8	13_8
No. 2	14_8	15_8	16_8	17_8

INSTRUCTION COMPLEMENT

General information on timing etc. is given in:-

(a) Doc No. 70130072167, H-316 Interface Manual.

(b) Doc. No. 130071732, DDP-416 Interface Manual.

(c) Doc. No. 130071624, DDP-516 Interface Manual.

OCP Instructions

OCP instructions are used to initiate motion of a device or prepare it for a special mode of operation and no response signal is expected from the device. Only the address bus lines and the command pulse (OCPLS-) are involved. The device address code and function code are transmitted from the OCP instruction word bits 07 through 16 to the corresponding bit positions of the address bus. The command pulse occurs during the latter half of the address interval to enable the addressed device to perform the function specified by the function code portion of the instruction. During this instruction any information placed by the device on DRLIN- or INB will be ignored by the CP.

The OCP instructions used with the Magnetic Tape Option are:-

OCP'001x	Sets the selected MTT in motion and instructs it to read in BCD two-characters-per-word mode.
OCP'011x	Sets the selected MTT in motion and instructs it to read in binary two-characters-per-word mode.
OCP'021x	Sets the selected MTT in motion and instructs it to read in binary three-characters-per-word mode.
OCP'031x	Instructs the TCU to set up the normal DMA/DMC mode.
OCP'041x	Sets the selected MTT in motion and instructs it to write BCD two-characters-per-word.
OCP'051x	Sets the selcted MTT in motion and instructs it to write binary two-characters-per-word.
OCP'061x	Instructs the TCU to write the end of file character.
OCP'071x	Instructs the TCU to reset the DMA/DMC mode.
OCP'101x	Sets the selected MTT in motion and instructs it to write binary three-characters-per-word.
OCP'111x	Instructs the selected MTT to space forward one record.
OCP'121x	Instructs the selected MTT to space forward one file.
OCP'131x	Instructs the TCU to set up DMA/DMC with auto switch.
OCP'141x	Instructs the selected MTT to rewind the tape.
OCP'151x	Instructs the selected MTT to space back one record.
OCP'161x	Instructs the selected MTT to space back one file.
OCP'171x	Instructs the selected MTT to stop writing.

SKS Instructions

SKS instructions are used to test the status of a device connected to the standard I/O bus. The instruction then looks for a status signal on DRLIN- within a prescribed interval. If an affirmative status signal is received within this time the next instruction is skipped. If no affirmative status signal is received the next instruction in the sequence is executed.

The SKS instructions used with the magnetic tape option are:-

SKS'001x	Enables the CP to skip the next instruction in the program if the TCU is ready to input a data word.
SKS'011x	Enables the CP to skip if the TCU is not busy.
SKS'021x	Enables the CP to skip if no error is detected.
SKS'031x	Enables the CP to skip if the beginning of the tape (BOT) is not detected.
SKS'041x	Enables the CP to skip if the TCU is not interrupting.
SKS'051x	Enables the CP to skip if the end of the tape (EOT) is not detected.
SKS'061x	Enables the CP to skip if the end of file (EOF) is not detected.
SKS'071x	Enables the CP to skip if writing is permitted.
SKS'111x	Enables the CP to skip if the MTT is operational.
SKS'121x	Enables the CP to skip if the DMA/DMC subchannels are not using channel 2.
SKS'131x	Enables the CP to skip if the DMA/DMC is not in the auto switch mode.
SKS'141x	Enables the CP to skip if the MTT not rewinding.

INA Instructions

The INA instructions are used to input data from the TCU to the 'A'-register via the input bus (INB) when reading. The device and function code of the INA instruction are sent out on I/O bus and a ready signal looked for on DRLIN-. If a ready signal is received within a predetermined time the content of the INB is logically ORed with the contents of the 'A'-register and the next instruction skipped. A reset ready signal is also sent out to inform the TCU that the data has been accepted by the CP. If a ready signal is not received no transfer takes place and the next instruction executed.

The INA instructions used with the magnetic tape option are:-

INA'001x	If a ready signal is received causes the information contained in the TCU buffer to be ORed into the 'A'-register and the next instruction is skipped. If no ready signal is received the next instruction is executed.
INA'101x	Clears the 'A'-register before the transfer occurs, otherwise this instruction is the same as INA'001x.

OTA'001x Instruction

The OTA'001x instruction is used to input data from the 'A'-register into the TCU buffer via the output bus (OTB) when writing. The device and function code are sent out on the I/O bus and a ready signal looked for on DRLIN-. If a ready signal is received the contents of the 'A'-register are entered into the TCU buffer and the next instruction is skipped.

SMK'0020 Instruction

This instruction sets the standard interrupt mask flip-flop. Each bit of the 'A'-register controls a device for SMK pruposes. TCU No. 1 is allocated bit 01 and TCU No. 2 bit 2 a one bit sets the mask and a zero resets it. When the interrupt mask is set interrupts can take place.

SECTION 4
THEORY OF OPERATION

GENERAL

The TCU module provides a means of compatible interchange of information between the MTT's and the computer I/O bus. The relationship between an MTT, the TCU logic and I/O bus is shown in simplified block diagram form in Figure 4-1. For the purpose of this manual the theory of operation is divided into three parts. These parts are:-

(a) General Theory, based on the simplified block diagram.

(b) Functional Theory, based on the logic block diagrams (LBD) at the rear of this manual.

(c) Operational Theory, which describes the various operations with the aid of timing diagrams, flow charts and analysis tables.

The TCU comprises eight main functional areas which are:-

(a) Address and control logic.

(b) Motion control logic.

(c) MTT, selection logic.

(d) MTT driver logic.

(e) Read control logic.

(f) Write control logic.

(g) Word forming buffer.

(h) DMC/DMA subchannel logic.

General theory and functional theory descriptions define the operations performed by each area. Their combined operations to perform the various TCU functions are described under Operational Theory.

Various indicators and switches on the MTT control panel are referred to in this section. For further detailed description refer to Section 1 of the Magnetic Tape Transport Manual, Doc. No. 42400343041.

GENERAL THEORY

Address and Control Logic

This logic is primarily concerned with accepting commands from the CP and converting them into signals which will initiated the desired operation. This logic also produces the device ready signal DRLIN- in response to SKS, INA and OTA instructions. The program interrupt request PIL00- is generated if the interrupt mask is set and the buffer control is ready. PIL00- is also generated at the end of operations by end of motion interrupt, EMINT+.

Motion Control Logic

The motion control logic receives the decoded CP commands from the address and control logic and uses them to generate signals which will initiate the desired motion and generate the motion busy status MBSYS+. Motion is implemented by forward, reverse and rewind flip-flops which are conditioned by the appropriate OCP commands. A delay is initiated by the motion signals which allows an MTT at rest to build up to normal operating speed before it is required to accept or furnish data.

Tape motion is terminated when an interrecord gap is detected by the read logic. The read control logic resets the motion control flip-flops and triggers a busy extension. At the end of this extension the TCU is ready to accept and execute another OCP command. Should this subsequent OCP require continued tape motion in the same direction it will be executed without disturbing tape motion. If however, motion is to be reversed the MTT is brought to rest before the command is executed.

At the end of write operations the end of record gap is detected by read after write logic which initiates a forward extension to ensure that the interrecord gap is correctly positioned with respect to the MTT read/write head assembly when motion ceases. Similarly there is a reverse extension.

A rewind command sets the rewind flip-flop and a 120 milli-second rewind command is initiated and sent to the MTT. The TCU then becomes available to execute OCP commands for another associated MTT.

MTT Selection Logic

Four similar sets of selection logic are employed, one for each MTT. The MTT selection logic generates the select MTT signals from the CP commands and signals derived from the address selector on the MTT. The address selector has eight positions numbered 0 through 7 of which positions 0 through 3 only are used. The selection logic also contains input transfer gates for data and control signals from the MTT.

MTT Driver Logic

The MTT driver logic contains data and control signal drivers which act as output buffers for signals from the TCU to each MTT. Selection signal from the selection logic ensure that these output signals are only applied to the selected MTT. To achieve this a separate set of drivers is employed for each MTT.

Read Control Logic

A write alignment signal generated by the MTT is used to generate read strobes which are synchronised with the TCU high or low density clock. Read strobes enter data read from tape into the word forming buffer. A five stage counter is incremented at four times the frame rate and synchronised by the read strobes. Since read strobes are not generated for gaps the counter is permitted to count down until its' output is correct for the generation of a gap detected pulse. Reading continues until the gap following the longitudinal parity character (interrecord gap). Detection of this gap causes the motion control logic to be reset terminating operations. Each character read from tape enters lateral and longitudinal parity checkers. Lateral parity checking is carried out on each character and longitudinal parity is checked when the longitudinal parity character is read at the end of the record.

Write Control Logic

The write control logic contains the high and low density clocks and frame rate clock circuits. The frequency and period of the clocks is a function of the densities at which the MTT's operate. When read or write enable conditions are set up in the TCU the clock output is divided down to produce the frame rate clock. The frame rate clock is synchronised with a write oscillator delay when writing from load point, or when writing an interrecord or file mark gap. Once the write oscillator delay has expired strobe pulses are generated to strobe data into the MTT.

Word Forming Buffer

The word forming buffer contains two 16-bit registers which provide a means of assembling 12-bit or 16-bit words from the 6-bit characters when reading, and enable the words to be broken down into characters when writing. Data read from tape produces the read strobe which enters the character into the rank one register (R1B) bit positions 01 through 06. The second character enters bit positions 07 through 12 in a similar manner. If in the three-characters-per-word mode the third character enters bit positions 13 through

16. The word thus assembled in R1B is transferred to the rank two register (R2B) which drives the input bus (INB) to the CP.

Data to be written on tape enters R1B via the output bus (OTB) or the DMA bus. The complete word is transferred to R2B and synchronised to the frame rate clock and write oscillator delay. The data is gated from R2B to the NRZ register one character at a time, and a lateral parity bit is generated for each character. The transfer to the NRZ register is controlled by write strobes which are functions of the frame rate clock. After transfer from R1B to R2B the R1B register is cleared and available for a new word from the CP. When the appropriate number of characters has been strobed into the NRZ register a transfer from R1B to R2B again occurs. This procedure continues until the entire record is written.

DMA/DMC Subchannel

The DMA/DMC subchannel permits the TCU to communicate with the CP by way of the DMA and DMC options. The DMA option responds to the TCU request line to furnish data from the CP to the TCU. The DMC option controls the execution of data transfers between the TCU and CP in response to program interrupt requests.

FUNCTIONAL THEORY

Address and Control Logic

Address Decoder - (LBD No. E010). The address portion of an instruction ADB11- through ADB16- is decoded to provide the magnetic tape address MTADD+ and MTT selection signals XXXX0+ through XXXX3+. In a double TCU configuration the condition of ADB14- determines which TCU is being addressed.

The function portion, ADB08- through ADB10- is applied to octal-to-binary decoder A44A which is enabled by MTADD+. If the instruction is not addressed to the TCU the decoder action is inhibited by MTADD+ which is not true. Function bit ADB07- is used to generate signals A1XXX+ and A1XXX- which are used in conjunction with output control pulse OCPLS+, MTADD+ and the output of gate B55C to generate AOCP0+ or AOCP1+. An address in which ADB07- is passive (+6 volts) causes A1XXX- to be passive (+6 volts) and A1XXX+ to be not true (0 volts). Gate A47C is enabled and AOCP0+ is generated. If ADB07- is active (0 volts) A1XXX+ is true (+6 volts), gate A47B is enabled and AOCP1+ is generated. Gate B55C has two inputs, MBSYS+ and A3V7X-. If the TCU is busy MBSYS+ is true (+6 volts) and operation of A47B and A47C is inhibited. A DMC/DMA or stop write command causes A3V7X- to go low and AOCP0+ or AOCP1+ may be generated.

The OR of AOCP0+ and AOCP1+ (A18L) generates CALLP+ which is used for the general resetting of flip-flops at an early stage enabling them to perform their tasks when called upon to do so. CALLP+ also enables the MTT selection logic and deactivates the PIL00- line (see motion control logic).

Control Logic - Function control signals AX0XX through AX7XX with AOCP0- or AOCP1+ define the operation to be performed. If this operation requires the two-characters-per-word mode the OR of four of these signals at gate A47E generates S2CPW+. The remainder of the operation definition is shown in the left hand half of LBD No. E011. The signals generated are shown with respect to the OCP initiating them in Table 4-1.

Table 4-1 Control Functions

OCP'	AOCP0+ or AOCP1+	AX0XX through AX7XX signal	OUTPUT	GATE	FUNCTION INITIATED
001x	AOCP0+	AX0XX-	S2CPW+	A47E	Set 2 character/word
			CRTEP-	A48B	Read
			CFWDP-	A43C	Forward
			CRERS+	A43A	Reset erase
			CWRDP-	A52K	Write or read
			CEVPP-	A48C	Even parity
011x	AOCP0+	AX1XX-	S2CPW+	A47E	Set 2 character/word
			CRTEP-	A48B	Read
			CFWDP-	A43C	Forward
			CRERS+	A43A	Reset erase
			CWRDP-	A52K	Write or read
021x	AOCP0	AX2XX-	CRTEP-	A48B	Read
			CFWDP-	A43C	Forward
			CRERS+	A43A	Reset erase
			CWRDP-	A52K	Write or read
041x	AOCP0+	AX4XX-	S2CPW+	A47E	Set 2 character/word
			CWRTP-	A52P	Write
			CFWDP-	A43C	Forward
			CWRDP+	A52K	Write or read
			CEVPP-	A48C	Even parity
			CWDAP-	A52M	Write data
051x	AOCP0+	AX5XX-	S2CPW+	A47E	Set 2 character/word
			CWRTP-	A52P	Write
			CFWDP-	A43C	Forward
			CWRDP+	A52K	Write or read
			CWDAP-	A52M	Write data
061x	AOCP0+	AX6XX+	CWFMP-	A48D	Write file mark
			CWRTP-	A52P	Write
			CFWDP-	A43C	Forward

Table 4-1 Control Functions (Cont)

OCP'	AOCP0+ or AOCP1+	AX0XX through AX7XX signal	OUTPUT	GATE	FUNCTION INITIATED
101x	AOCP1+	AX0XX+	CW3BY- CWRTP- CFWDP+ CWRDP- CWDAP-	A46H A52P A34C A52K A52M	Write 3 binary Write Forward Write or read Write data
111x	AOCP1+	AX1XX+	CFWDP+ CRERS+	A43C A43A	Forward Reset erase
121x	AOCP1+	AX2XX-	CSFMP- CFWDP+ CRERS+	A48E A43C A43A	Search file Forward Reset erase
141x	AOCP1+	AX4XX+	CRWDP+ CRERS+	A52L A43A	Rewind Reset erase
151x	AOCP1+	AX5XX-	CREVP+ CRERS+	A52N A43A	Reverse Reset erase
161x	AOCP1+	AX6XX-	CSFMP- CREVP+ CRERS+	A48E A52N A43A	Search file Reverse Reset erase
171x	AOCP1+	AX7XX+	CRINT+	B44D	Control ready interrupt

The logic in the right hand half of LBD No. E011 generates the device ready signal is in response to SKS, INA and OTA commands and the ready line becomes active (0 volts) when the condition required by the command is true. The instruction generate signals AX0XX through AX7XX which are ANDed with the required status signal to drive DRLIN- to ground.

Signal MTINT- becomes active (0 volts) when the interrupt mask flip-flop (B32C) is set as a result of an SMK'0020 instruction and MTMSK+ is true, the word forming buffer is ready (BCRDY+ true), the TCU is not in the DMA/DMC mode (DMCMF- passive) and the control ready interrupt flip-flop is reset (CRINT- passive). MTINT- grounds the PIL00- line for program interrupt requests and provides interrupt status for SKS'041x. Interrupts are also performed at the end of operations when EMINT+ makes MTINT- active.

Motion Control Logic

The motion control logic which is all contained in LBD No. E013 uses the motion commands from the address and control logic to initiate motion of the selected MTT. The logic contains a delay which enables an MTT at rest to build up to normal operating speed before data transfers are allowed.

A forward command CFWDP+ sets the forward flip-flop (A37C) and resets the motion reverse history flip-flop (B45F). With A37C set MFWDF+ is true and is applied to gate A41E where it is ANDed with the OR of MHOLD and MWELF+ AND SWPER- to generate FWDCM+ and SYSRG+ at gates B46G and A57F respectively. The forward command is inhibited if the motion hold flip-flop is set or if writing is permitted. Signal FWDCM+ is the forward enable signal for all four MTT's and allows the drive logic to apply a forward command to the selected MTT. Signal SYSRG+ triggers delay multivibrator B51B to generate AUXCP+ which triggers B41B to reset the read block flip-flop. This is the delay which allows the MTT to build up to speed. Motion busy status MBSYS+ is raised by MFWDF- at gate A38F to inhibit AOCP0+ or AOCP1+ and to indicate the motion busy status for SKS'011x.

A reverse command CREVP+ sets the reverse motion (B48A) and motion reverse history (B45F) flip-flops. With B48A set MREVF+ is true and is ANDed with MHOLD- at gate A41F to generate REVCM+(B46H), and SYSRG+ (A57F). Signal REVCM+ is the reverse enable signal for all four MTT's and allows the driver logic to apply a reverse command to the selected MTT. Motion busy status MBSYS+ is raised by MREVF- and acts as described in forward motion. MREVF+ also enables the reverse extension delay multivibrator (B31A) which is triggered at the end of operations (RCEOP+) to generate REVEX- which sustains MBSYS+ for a further 8 milli-seconds after the operation is terminated.

Forward and reverse commands reset or set the motion reverse history flip-flop (B45F) respectively. The motion command of a subsequent OCP is compared with the condition of B45F at gates B42E and B42H. If this OCP requires a change of direction delay multivibrator A21B is triggered to set the motion hold flip-flop (B48C) and MHOLD- inhibits the execution of the command. If this OCP requires that motion continues in the same direction A21B is not triggered and the MHOLD flip-flop remains reset. MHOLD- allows the command which is sent to the MTT before it comes to rest.

Rewind command CRWDP+ sets the rewind flip-flop (B48B) and RWDCM+ becomes true. RWDCM+ is the rewind enable signal for all four MTT's and allows the driver logic to apply a rewind command to the selected MTT. It also enables triggering of the rewind

extension delay multivibrator B57A and triggers B51B to generate AUXCP+. This triggers B57A to initiate the extension and B41B to reset the read block flip-flop (B32B). Motion busy status is raised by RWDCM- at gate A38F. When the 120 milli-second extension has expired B48B is reset and the TCU is initialised. If the tape is completely rewound before the extension expires load point signal STLDP- becomes active to terminate the operation.

When an OCP is issued CALLP+ resets B45A and B45B flip-flops and EMINT+ becomes not true to deactivate PIL00- from the last end of motion interrupt. The reset output of B45B acts as a set level for the four device busy flip-flops (B47A, B47B, B47C and B47D). The three flip-flops corresponding to MTT's not selected remain reset due to their selection signals (SELTx+) remaining not true. The flip-flop corresponding to the selected MTT is set when MBSYS+ becomes not true to generate the device busy status (xBUSY+). MYSYS+ becoming not true also triggers B41A which generates BSYEX+ to reset the device busy flip-flop after 8 milli-seconds. The device busy status is used to generate SBUSY- which enables the motion hold flip-flop (B48C) to be set if another OCP is sent out during the duration of xBUSY+.

When an operation is completed signal RCEOP+ is generated by the read control logic. RCEOP+ at gate B42K generates MREST+ which resets the forward or reverse motion flip-flop as appropriate to halt tape motion. When write operations are terminated however, the resetting is delayed for 3.75 milli-seconds by forward write extension FWREX- (B31B). The motion busy status is sustained for a further 8 milli-seconds when terminating reverse operations by reverse extension REVEX- (B31A).

MTT Selection Logic

Four similar MTT selectors are employed, one for each MTT. Selection is achieved by gating the selection commands XXXX0+ through XXXX3+ with functions of the tape address selector on the MTT control panel, TxAD0+ through TxAD3+.
For example:- MTTA dialed to 0 and the CP command requires selection of MTTA. Signal TAAD0+ is true and XXXX0+ is also true. Signal AADDC+ (LBD No. E014) becomes true and CALLP+ enables the set level to the select flip-flop (C24C) and SELTA+ becomes true with PLUP6+. Inputs to MTTB, MTTC and MTTD selection logic (LBD Nos. E015, E016 and E017) are such that BADDC+, CADDC+ and DADDC+ are all not true and their selection flip-flops are reset. SELTA+ is the enable signal for control and data signals between the TCU and MTTA.

The selection logic also contains input transfer gates for control and data signals from the MTT. Two sets of data gates are included to enable determination of high or low tape channel error. Control signal TALNH+ informs the TCU whether a high or low error has been committed. If a low error exists the low not high error flip-flop in the read control logic sets and LNHEF+ generates SALOC+. No such error causes the LNHEF flip-flop to remain reset and LNHEF- generates SAHIC+. Signals SALOC+ and SAHIC+ determine which set of data transfer gates allow the data into the word forming buffer.

When the MTT is operational it generates head in position signal TxHIP- which produces SREDY-. This is the MTT operational signal for SKS'111x. An MTT which is set up for writing generates permit signal TxPER+ from which SWPER- is derived for write permit SKS'071x purposes.

A tape which is at the load point marker causes the MTT to generate signal TxBOT+ which generates STLDP-. This informs the TCU that a load point gap follows and is used to generate DRLIN- in response to an SKS-031x instruction. Similarly the MTT generates TxEOT when the end of tape marker is generated. This produces signal STEOT- which sets the end of tape flip-flop in the motion control logic to make EOTSF- active (0 volts). An SKS'051x instruction issued when the end of tape marker is not detected (EOTSF-passive) drives DRLIN- to ground.

MTT Driver Logic

The MTT driver logic (LBD No. E018 through E021) comprises four similar sets of output drivers, one to each MTT. Seventeen power amplifiers are employed in each to drive the write data and control lines from the TCU to the MTT. The logic is enabled by MTT selection signals (SELTx+) to ensure that data and control signals are applied to the selected MTT only.

An erase flip-flop is set by CWRTP+ and xADDC+ to enable the erase head when writing. When other operations are being performed the erase flip-flop is reset by CRERS+ and xADDC+ to disable the erase head.

A rewind status flip-flop is set by the AND of rewind command RWDCM+ and the MTT select signal SELTx+ to establish the rewind status SRWDS- for SKS'141x. This remains set after the 120 milli-second duration rewind enable RWDCM+ to sustain the rewind status. The rewind status flip-flop is reset by head in position signal TxHIP-.

Read Control Logic

Read Control - The read control is shown in LBD No. E023. The read flip-flop (A31A) is set by read command CRTEP- and READF+ becomes true. Read signal READF+ conditions the buffer control for reading and enables the read drop in pulse RCDIP+, and external stop signal EXSTP- to be generated. The read or write level RCRWL+ is derived from READF-.

Low not high tape channel error signal SLNHE- from the selection logic is ANDed with RDBLK- and if a low error exists SLNHE+ is true and sets the low not high error flip-flop (A13F). LNHEF+ becomes true to strobe the low channel data into the selection logic. If there is no such error the error flip-flop remains reset and the high channel data is allowed by LNHEF-.

Read Strobe - When a character is read from tape the OR of the read amplifiers in the MTT generates TxWAT+ from which write alignment pulse STWAT+ is derived. The alignment pulse STWAT+ is ANDed with RDBLK- and NTRES- at gate A14C (LBD No. E024) to ensure that reading is allowed and that the previous character has been stored in the word forming buffer. The collection delay (A21A) is triggered and COLLD+ sets the no trespass flip-flop (A18D). NTRES+ triggers the read strobe delay (A11B) to generate read strobe RSTRB+ at B28C. When reading RSTRB+ strobes the data into the longitudinal parity checker (LBD No. E022), enables the file mark detector (LBD No. E023), generates drop in pulse RCDIP+ and resets the low not high error flip-flop if set (LBD No. E023). Read strobe RSTRB+ also enables the gap counter by setting gap counter enable flip-flop (A18E) (LBD No. E024). When writing RSTRB+ is generated to enable parity checking and gap detection.

The read drop in pulse RCDIP+ (LBD No. E023) is the function of RSTRB+ which is used to control data transfers within the word forming buffer. The drop in pulse is enabled by motion not reverse MREVF-, gap not detected RGDET- and reading allowed READF+ which ensure that the TCU is in the correct mode for read data transfers.

Input Data Character - (LBD No. E022). The high or low channel data from the selection logic is ORed to produce data signals STRB1 through STRB7. Data bits STRB2+ and STRB4+ are used to generate character conversion signals RDDB2+ and RDDB4+ for code conversion from octal 12 to octal 00 when reading BCD.

Longitudinal Parity Checker - (LBD No. E022). Data signals STRB1+ through STRB7+ are strobed into the longitudinal parity checker by RSTRB+. The checker comprises a 7-bit register each bit position of which changes state for a one bit from the corresponding tape channel. After the longitudinal parity character is read the register must be all reset. This means that the check bit for each track corresponds with what was written on tape and provides a confidence level for the authenticity of the record. If any bit position remains set after the parity character is read RSPEF- sets the parity error flip-flop to generate PARCK-.

Lateral Parity Checker - (LBD No. E022). Data signals STRB1+ through STRB6+ with their inversions are applied to the lateral parity exclusive OR pyramid and the result compared with STRB7+ and STRB7-. The parity status thus produced is compared with the condition of the even parity flip-flop (see output data character). With even parity selected CEVEN+ is true and an error causes the inputs to gate A28F to be such that RSPEF- is generated to set the parity error flip-flop.

Gap Detection - The TCU high or low density clock is enabled during read operations and used to increment the gap counter at the clock rate (WCCLK+) which is four times the frame rate. When RSTRB+ occurs and sets A18E (LBD No. E024) the gap counter set synchronised level flip-flop (A16C) is set and RGSSY+ sets the gap counter enable flip-flop (A18F). The gap counter is initially set to octal 37 by RGSSY-, which also resets A18E. If no further read strobe occurs within six counts the inputs to gate A15E are such that RGAPD+ occurs. A further read strobe within the six count period however forces the counter back to octal 37. If the MTT is moving across a no data gap RGAPD+ sets gap detected flip-flop A18A and RGDET+ becomes true to set A18B if a further read strobe occurs. If the gap is genuine the count continues until end of record signal RCEOR+ is generated (A17N) to reset the gap counter enable flip-flop and A18B which has no further effect. If the gap is due to dirty or defective tape and another RSTRB+ occurs before RCEOR+ error signal RSPEF- is generated at gate A34K to set the parity error flip-flop.

End of record gap detected signal RCEOR+ is used to halt tape motion by generating an end of operation signal RCEOP+ (LBD No. E023). The read control search for file mark flip-flop (A13E) is reset under normal read/write operations and RCSFM- is passive (+6 volts). The AND of RCSFM- and RCEOR+ at gate A27E generates RCEOP+ which in turn generates MREST+ to halt tape motion.

File Mark Detection - (LBD No. E023). Search for file mark signal CSFMP- from the address and control logic sets the read control search for file mark flip-flop (A13E) and RCSFM+ is true. A file mark is detected by the AND of STRB1+ through STRB4+, STRB5- through STRB7-, RSTRB+ and RGCEN-. Signal RGCEN- ensures that a character containing octal 17 which is part of a record is not treated as a file mark. The resulting signal sets the file mark detected (A13B) and A13C flip-flops. With A13B set RCFMD+ is true and in conjunction with RCEOR+ and RCSFM+ generates RCEOP- at gate A14B. Signals RCFMD+ and RCEOR at gate A27C also set the end of file flip-flop (A13D) to make RCEOF+ true. The condition of the end of file flip-flop can be tested with an SKS'061x instruction. With the flip-flop reset RCEOF- is passive and drives DRLIN- to ground enabling the CP to skip.

Write Control Logic

Write Control Clock - The clock circuit contains the high and low density clocks (LBD No. E025). Depending upon the position of the high/low density switch on the MTT either the high (B34A), or low (B37A) density clock is enabled. Signal STLOD- is the function of the density switch and enables the appropriate clock. With the high density clock enabled the clock output WHICK- (284.2 kHz) is divided by eight (B23F, B23A, B23B) to generate the write control clock WCCLK-. If the low density clock is enabled its' output WLOCK- (204.2 kHz) is divided by sixteen (B45E, B23C, B23D, B23E), to generate WCCLK-. The frame rate clock WCFRK+ is obtained by dividing WCCLK- by four (B44E, B44F).

Write Control - The write order from the address and control logic CWRTP+ sets the write enable flip-flop (A37B) (LBD No. E026) and MWELF+ becomes true to generate the MTT write enable signal WRITE+. This is the write enable level for all four MTT's and enables the driver logic to apply it to the selected MTT. When the MTT is in motion the AND of MHOLD+ and MWELF+ generates WOSDT- to trigger the write oscillator delay (B21A, B21B). The write oscillator delay period of 30.6 milli-seconds provides a $\frac{3}{4}$ inch interrecord gap (NORMAL GAP). To generate a file mark gap the write file mark command CWFMP- sets the write control write file mark flip-flop (B45D) (LBD No. E025) and WCWFM+ is true. WCWFM- inhibits the normal gap logic and triggers the write oscillator delay. The write oscillator delay output is divided by eight (B38A, B38B, B38C) (LBD No. E026) to provide a delay period of 244.8 milli-seconds

which provides a gap of approximately 3.7 inches. When writing from load point STLDP+ is true and in conjunction with AUXCP+ (B27H) sets the write at load point flip-flop (A37E). MWLDP- triggers the write oscillator delay and inhibits the normal gap logic. MWLDP+ enables the divide by sixty four circuit (B38A, B38B, B38C, B38D, B38E, B38F, A37E) which provides a delay period of approximately two seconds to provide a gap of 35 inches.

When the appropriate gap delay has expired the OR of the gap signals set A37D which in turn sets the write strobe enable flip-flop (B32D) and MWSEN+ becomes true. Write strobe enable level MWSEN+ enables normal write strobes WCNWS- for normal write mode, write file mark strobe WCFMS- for write file mark and write reset pulse WCWRP- for write longitudinal parity character.

<u>Write Strobes</u> - The normal write strobe WCNWS- is generated at gate B43F (LBD No. E025) by the AND of MWSEN+, WCFRK, WCWFM- and BXFCF-. Signal WCWFM- is passive (+6 volts) under normal write conditions and inhibits WCNWS- if writing a file mark. BXFCF- is the function of the buffer transfer control flip-flop which is reset when MWSEN+ occurs (see buffer control) and is passive (+6 volts) to allow writing. The normal write strobe WCNWS- triggers the write pulse delay multivibrator (B45B) which in turn triggers B51A to generate a 5.5 micro-seconds duration write pulse WRTPL+. This is the write pulse for all four MTT's and allows the MTT driver logic to apply a write pulse to the selected MTT. Signal WCNWS- also clocks the buffer character distributor to place the character to be written into the NRZ register. The data is strobed into the NRZ register by the inversion WCNWS+

The write file mark strobe WCFMS- is generated at gate B43E by the AND of MWSEN+, WCFRK+, WCWFM+ and WCFSS-. Signal WCWFM+ is true when writing a file mark and WCFSS- is passive until the file mark strobe has been generated. WCFMS- occurs with WCFRK+ and sets the file strobe storage flip-flop (B45C) and WCFSS- becomes active to inhibit any further WCFMS-. The file mark strobe also triggers the write pulse delay to generate write pulse WRTPL- and sets NRZ register bits 02 and 03. Write seven track file mark signal W7TFM- is derived from WCFMS+ to set the NRZ register bits 01 and 04.

<u>Longitudinal Parity Character</u> - When a record is complete the longitudinal parity character is written on tape. Write strobe pulses are generated at gate B43C by the AND of MWSEN+, WCFRK+, WCWFM- and BXFCF+ if the character follows a record. If the longitudinal parity character follows a file mark the write strobe is

generated at gate B43D by the AND of MWSEN+, WCFRK+, WCWFM+ and WCFSS+. The resultant strobe pulses are applied to divide by four circuit B44A and B44B to generate WCWRP-. Signal WCWRP- triggers the write pulse delay to generate WRTPL- and resets the NRZ register. The inversion resets the write file mark flip-flop (B43D) if it is set, the file mark strobe storage flip-flop (B45C) and the write strobe enable flip-flop (B32D) (LBD No. E026) to prevent any further write strobes.

When write operations are completed the read after write logic terminates the operation by generating RCEOP+ which in turn generates MREST+. Signal MREST resets the write enable flip-flop and MWELF- triggers B56A (LBD No. E026) to sustain WRITE+ for a further 8 milli-seconds.

Word Forming Buffer

The word forming buffer comprises the Rank 1 Register (R1B) (LBD No. E028), the Rank 2 Register (R2B) (LBD No. E029), data formatting logic (LBD No. E030), a lateral parity bit generator and NRZ register (LBD No. E031) and the buffer control logic (LBD No. E027).

Rank 1 Buffer - This is a 16-bit parallel entry register which accepts data from the output bus (OTB) in the write mode, and from the input data character logic (LBD No. E022) in the read mode. When writing the complete word is received and strobed into the register by BTTOE+. Data read from tape is accepted character serially. The first character is strobed into bit positions R1B01 through R1B06 by BCSC1+, the second into bit positions R1B07 through R1B12 by BCSC2+ and the third, if in the three character per word mode, into R1B13 through R1B16 by BCSC3+. When the word has been transferred to R2B signal BCRES- occurs to reset R1B in readiness for the next word in the record.

Rank 2 Buffer - This is also a 16-bit parallel entry register which accepts complete data words from R1B. These inputs are strobed into R2B by transfer signal BXFER+. In the write mode the data transfer to the MTT is through the data formatting logic. Data which has been read is strobed onto the input bus (INB) by transfer signal BEINB+.

Output Data Formatting - Because the MTT only accepts data character serially the contents of R2B must be broken up and a lateral parity bit generated when writing. This is performed by the data formatting logic (LBD No. E030) under the control of the

buffer control logic. The buffer control issues control signal BCEC1+ to strobe data bits R2B01+ through R2B06+ to the NRZ register, BCEC2+ for bits R2B07+ through R2B12+ and if in the three characters per word mode BCEC3+ for bits R2B13+ through R2B16+. These transfer control signals are functions of the normal write strobe WCNWS+ and occur sequentially at one frame intervals.

Output Data Character - The formatted data is applied to the NRZ register and lateral parity bit generator simultaneously. The NRZ register is a 7-bit register with input gating. When in the BCD mode character conversion from 00_8 to 12_8 is performed by comparison gating (A31E, A31D, A34C, A34D). The data present at the input gates is strobed into the NRZ register by normal write strobe WCNWS+. When a file mark is to be written signals W7TFM- and WCFMS- are set levels for bits WDAT1+ through WDAT4+. At the end of each record and after a file mark the write reset pulse WCWRP- occurs and resets the NRZ register. The final character thus generated is the longitudinal parity character and is written four frame spaces later.

The lateral parity generator comprises an exclusive OR pyramid similar in operation to the lateral parity checker, and the parity selection flip-flop (A37A). This selection flip-flop is set (CEVEN+ true) when in the BCD mode (even parity) and reset in the binary mode (odd parity). The condition of this flip-flop is compared with the number of one bits in the character. The parity bit thus generated is applied to the WDAT7+ position of the NRZ register.

Signals WDAT1+ through WDAT7+ are the write data signals for all four MTT's and enable the MTT driver logic to apply them to the selected MTT.

Buffer Control - The buffer control logic (LBD No. E027) controls the transfers of data in the word forming buffer in both read and write modes. A read or write OCP generates read or write signal CWRDP- which initialises the transfer control by setting B35B and resetting B35C and B35D.

The buffer is placed in the two or three-character-per-word mode by B35A flip-flop. A two-character-per-word OCP generates S2CPW+ which in conjunction with AOCP0+ sets B35A to make B2CPW+ true. This enables generation of the last character time two-characters-per-word signal LCT2C+ (A12M) and buffer control last character time single BCLCT+ (A35H). An OCP which requires the three-characters-per-word mode generates AX2XX+ to reset B35A. B2CPW- is passive (+6 volts) to enable BCLCT+ and buffer character three time BCH3T+.

When reading in the two-characters-per-word mode the first character generates RCDIP+ to trigger delay multivibrator A11A to produce a strobe pulse which clocks the transfer control. B35B resets, B35C sets and B35D remains reset. The B35B function BCEC1+ at gate B26J generates BCSC1+ in conjunction with RCDIP+ to strobe the first character. With B35C set BCHD2+ is true and generates LCT2C+ and BCLCT+. The RCDIP+ corresponding to the second character sets B35B and resets B35C. The BCEC2+ function of B35C at gate B26K generates BCSC2+ in conjunction with RCDIP+ to strobe the second character. The inversion of RCDIP+ in conjunction with BCLCT+ at gate B27A causes the input to B28A to go low to produce BXFER+ which transfers the word from R1B to R2B and sets the ready flip-flop (B32A).

In the read three-characters-per-word mode the first and second characters are transferred as described above. The second RCDIP+ sets B35D and resets B35C and generates BCSC2+. With B35D set BCLCT+ and BCH3T+ become true. The RCDIP+ corresponding to the third character sets B35B and resets B35D. The BCEC3+ function of BCH3T+ at gate B26P generates BCSC3+ in conjunction with RCDIP+. The inversion of RCDIP+ in conjunction with BCLCT+ at gate B27A generates BXFER+ as before.

Transfer signal BXFER strobes the word assembled in R1B into R2B, and sets the ready flip-flop (B32A). Signal BCRDY+ becomes true to inform the CP that data is ready for transfer. The last character time signal BCLCT+ at gate B55E generates RESR1- which in turn generates BCRES- (B28D) to reset R1B ready for the next word.

The CP senses the ready condition by means of an SKS'001x instruction, or the PIL00- line if the interrupt mask is set. The CP executes an INA'001x or INA'101x which generates MTADD+ and drives RRLIN- to ground. The AND of RRLIN+ and MTADD+ at gate A47A produces RRLAX- which resets the ready flip-flop. Magnetic tape address MTADD+ in conjunction with READF+ generates BEINB+ (B28F) to gate the contents of R2B onto the input bus (INB).

A write OCP instruction sets the buffer character distributor in similar manner to read commands. The write function CWDAP- sets the buffer control flip-flop (B48D) and BXFCF+ becomes true. CWDAP- also sets the ready flip-flop (B32A) to inform the CP that the TCU is ready to accept a word. BCRDY+ is also ANDed with write enable, MWELF+, at gate B27B to generate RESR1- to reset R1B. The CP senses BCRDY+ by means of SKS'001x, issues an OTA'001x instruction to generate MTTAD+, and drives RRLIN- to ground. The AND of RRLIN+ and MTADD+ generates RRLAX- (A47A) which resets the ready flip-flop. These signals are also ANDed with MWELF+ to produce RRLAO- (A38A) which in turn generates BTTOE- (B28E) to strobe the data on the output

bus (OTB) into R1B. The inversion RRLAO+ in conjunction with BXFCF+ triggers A11A to generate BXFER+ (B28A) which transfers the data word from R1B to R2B and sets the ready flip-flop once again. The trailing edge of BXFER+ in conjunction with MWSEN- resets the buffer control flip-flop to make BXFCF+ not true. RESR1- is generated as before to clear R1B ready for the next word. When the write oscillator delay has expired and MWSEN+ becomes true the write control logic generates normal write strobe pulses WCNWS-. The buffer character distributor is clocked by WCNWS- and action is similar to that for reading. Data is strobed character serially through the formatting logic by BCEC1+, BCEC2+ and BCEC3+ for entry into the NRZ register. Last character time signal BCLCT+ which becomes true with the last character transfer of each word generates subsequent transfer signal BXFER+. This allows the next word in R1B into R2B, clears R1B and sets the ready indicator thus preparing the buffer for the next word. When the last word in a record has been transferred BCRDY+ remains true because no further OTA'001x has been performed. The last character time signal BCLCT+ for the last character generates BXFER+ and the buffer control flip-flop (B48D) sets and BXFCF+ becomes true to enable the longitudinal parity character to be written.

DMC/DMA Subchannel

The DMC/DMA subchannel enables the TCU to communicate with the CP via the DMC option or the DMA option. The DMC/DMA subchannel logic is shown in LBD No. E012.

The normal DMC/DMA mode is set up by an OCP'031x command from the CP which generates AX3XX+ and AOCP0+. The AND of these signals grounds SDMCN- which sets flip-flop A54D, A54E to make DMCMF+ true. SDMCN- also resets the auto switch flip-flop (A53D) and DAUTO+ in turn resets the CHANB flip-flop (A53A) restricting interrupts to channel A. Normal interrupt requests are inhibited by DMCMF- which disables the PIL00- line. CALLP- derived from AOCP0+ resets A53C to make DERLF+ not true. The read or write function CWRDP- from the OCP instruction which set the TCU in operation resets A53B to make EXSPF+ not true.

The auto switch DMC/DMA mode is set up by an OCP'131x command which generates AX3XX+ and AOCP1+. The AND of these signals at gate A55B grounds SDMCA- to set the DMCMF+ flip-flop and the auto switch flip-flop. DAUTO+ provides set and reset control levels for the CHANB flip-flop which is clocked by end of range function DERLX+. With automatic subchannel switching thus in effect the CHANB flip-flop is toggled by DERLX+ each time end of range is reached. This feature is useful for processing gapless tapes.

Data interrupts DILXX+A for DMC and DILAX-A for DMA are produced on channel A by the AND of DMCMF+, BCRDY+, CHANB- (passive) and ENDXM- at gate A54B. Channel B interrupts DILXX+B and DILAX-B are produced similarly at gate A54A with channel B selected (CHANB+ true).

Operation of the DMC option is described in the Data Multiplexed Control Option Manual Doc. No. 130071647. Similarly DMA operation is described in the Direct Memory Access Option Manual Doc. No. 130071649.

The DMC/DMA modes are reset as a result of an OCP'071x command from the CP. The command generates signals AX7XX+ and AOCP0+ the AND of which at gate A55C ground REDMC-. This resets the DMCMF flip-flop, the DAUTO flip-flop and the CHANB flip-flop to initialise the subchannel logic.

OPERATIONAL THEORY

This part of the theory of operation describes the various operations with the aid of timing diagrams, flow charts and analysis tables. The mnemonics outside the flow chart boxes are the signals which implement the operation in the box.

Read Theory

The read BCD/Binary two-characters-per-word operation shown in timing diagram Figure 4-2 and flow chart Figure 4-4 is described in full. The read Binary three-character-per-word operation is similar and only the differences are pointed out.

Read One BCD/Binary Record Two-Characters-Per-Word - Operation is initiated by OCP'001x (BCD) or OCP'011x (Binary) command from the CP. Initialisation comprises selecting the required MTT (SELTx+), setting up for tape reading (CRTEP-, CWRDP), formatting tape data at two-characters-per-word (S2CPW+) and setting the parity network to read even for BCD or odd for Binary (C EVPP-). The PIL00- line is deactivated by CALLP+ which resets B45A and B45B to make EMINT+ not true. Reset erase signal CRERS+ resets the erase flip-flop of the selected MTT to disable the erase head. Forward motion is initiated by CFWDP+ which sets the forward flip-flop and resets the motion reverse history flip-flop. Signals MBSYS+, FWDCM+ and SYSRG+ are derived from the forward flip-flop function MFWDF+ to establish motion busy status, set the MTT in motion and trigger the read block delay (AUXCP+) which resets the read block flip-flop, RBLKF-.

When the first character passes under the read head STWAT+ is generated to initiate the 20 micro-second collection delay which allows some latitude in the time available to read each track of the character. At the end of the collection delay COLLD+ sets the no trespass flip-flop to trigger the read strobe delay RSDLY-. This generates the read strobe RSTRB+ to enter the character into the lateral and longitudinal parity checkers. RSTRB+ generates RCDIP+ which clocks the buffer character distribution and generates BCSC1+ to strobe the character into R1B. The read strobe also produces RGSSY+ which initiates the gap counter logic and generates read reset signal RDRES+ to reset the MTT read logic. The no trespass flip-flop resets with the trailing edge of RGSSY+ to enable the next read strobe. The second character is processed in similar manner and entered into R1B by BCSC2+. The 12-bit word thus assembled in R1B is transferred to R2B by BXFER+ which also sets the ready indicator (BCRDY+) to activate PIL00- if the interrupt mask is set. The R1B register is reset by BCRES+ready to accept the next word from the MTT. The CP executes an SKS'001x to test the ready condition followed by an INA'001x or INA'101x. The contents of R2B are allowed onto the input bus (INB) by BEINB+ and the ready indicator reset by RRLAX-.

The read cycle is repeated for each word in the record until a no data gap is detected and RGAPD+ occurs to set the gap detected flip-flop (RGDET+). The longitudinal parity character is read and entered into the longitudinal parity checker by RSTRB+ which also enables RGDET+ to set the parity error flip-flop should another read strobe occur before the end of record gap is detected.

When the end of record gap passes under the read head the gap counter is decremented until end of record signal RCEOR+ occurs. RCEOR+ resets the RGDET+ flip-flop and generates end of operation signal RCEOP-. This in turn generates motion reset MREST+ which resets the forward motion flip-flop to disable the forward command. The motion busy status MBSYS+ becomes not true to trigger the busy extension BSYEX+ and generate end of motion interrupt EMINT+.

<u>Read One Binary Record Three-Characters-Per-Word</u> - In this mode initiated by OCP'021x the TCU buffer transfer distributor is conditioned to accept binary data packed at three-characters-per-word. The two-characters-per-word flip-flop resets with AX2XX+ and AOCP0+. This sets the distributor to strobe a third character into R1B before initiating transfer signal BXFER+. Lateral parity is odd and there is no character code conversion. Due to word construction this mode can only be used to read tapes prepared on 16-bit compatible systems.

Write Theory

The write BCD/Binary two-characters-per-word mode shown in timing diagram Figure 4-3 and flow chart Figure 4-5 is described in full. The Binary three-characters-per-word mode is similar and only the differences are pointed out.

Write One BCD/Binary Record Two-Characters-Per-Word - The operation is initiated by OCP'041x (BCD) or OCP'051x (Binary) command from the CP. Initialisation comprises selecting the required MTT (SELTx+), setting the buffer control ready flip-flop, setting the buffer transfer control flip-flop (CWDAP), formatting tape data at two-characters-per-word (S2CPW+) and setting the lateral parity network to even for BCD or odd for Binary (CEVPP-). The PIL00- line is deactivated by CALLP+ which resets B45A and B45B to make EMINT+ not true. Write OCP function CWRTP+ sets the write enable flip-flop and the erase flip-flop for the selected MTT. Write enable, MWELF+ in conjunction with BCRDY+ generates RESR1- which in turn generates BCRES- to reset R1B. Forward motion is initiated by CFWDP+ which sets the forward flip-flop and resets the motion reverse history flip-flop. Signals MBSYS+, FWDCM+, and SYSRG+ are derived from the forward flip-flop function MFWDF+ to establish the motion busy status, set the selected MTT in motion and trigger the read block delay (AUXCP+) which resets the read block flip-flop (RBLKF-). Signal AUXCP+ in conjunction with MWELF+ generates WOSDT- to trigger the write oscillator delay.

The CP detects the ready status, BCRDY+ by means of an SKS'001x and executes an OTA'001x to transfer a complete word. Reset ready, RRLIN- from the CP generates RRLAX- to reset the ready indicator. RRLAO- is also a function of RRLIN- and generates BTTOE+ to enter the word into R1B, RRLAO- is also used in conjunction with BXFCF+ to generate BXFER which transfers the data from R1B to R2B. The trailing edge of BXFER+ resets the BXFCF flip-flop and sets the ready indicator. The R1B is reset as before and the CP may execute a second OTA'001x to transfer a second word to the buffer. Because BXFCF+ is no longer true BXFER+ is not generated as a function of RRLAO- and this word remains in R1B.

Depending on the position of the high low density switch on the MTT either the high or low density clock is enabled by STLOD-. For description purposes it is assumed that the high density clock is enabled (WHICK-). This frequency is divided by eight to produce the frame rate clock WCFRK+. When the write oscillator delay has expired to write strobe enable flip-flop (MWSEN+) sets to enable the normal write strobes, WCNWS-. The write strobes trigger the write pulse delay (WRTPL+) and clock the buffer character

distributor. Initially BCHD1+ is true and BCHD2+ is not true. The first character is strobed through the formatting logic by BCEC1+ and into the NRZ register by WCNWS+. The first write strobe resets BCHD1+ and sets BCHD2+. BCEC1+ becomes not true and BCEC2+ becomes true to strobe the second character into the formatting logic. BCHD2+ causes BCLCT+ to become true and the second write strobe sets BCHD1+ and resets BCHD2+. BCLCT+ in conjunction with WCNWS- also generates BXFER+ to transfer the next word from R1B to R2B. The ready indicator sets with BXFER+ as before to initiate the resetting of R1B, and the next word transfer from the CP.

The write cycle is repeated for each word in the record until there is no further OTA'001x command. BCRDY+ remains true and in conjunction with BXFER+ sets the buffer control flip-flop when one word time has elapsed. This disables the normal write strobe logic and enables the write reset pulse four frame spaces from the last character. Write reset pulse WCWRP- resets the NRZ register to generate the longitudinal parity character and triggers WRTPL-. If a file mark is to follow the record the write file mark exit is enabled by an OCP'061x command at this point

Read after write logic detects the end of record gap and RCEOR+ halts tape motion as when reading. The forward write extension FWREX- ensures that the interrecord gap is properly positioned with respect to the read/write head when the motion ceases. End of motion interrupt is generated to inform the CP that the TCU is available for further OCP commands.

Write One Binary Record Three-Characters-Per-Word - The operation is initiated by OCP'101x and the TCU conditioned to receive data in the 16-bit three-characters-per-word format. The two-characters-per-word flip-flop is reset by AX2XX+ enabling the character distributor to transfer three characters into the NRZ register before BXFER+ is generated.

Write End of File

The write end of file operation shown in flow chart Figure 4-6 is initiated by an OCP'061 command from the CP. Initialisation comprises selecting the required MTT (SELTx+), setting the write control write file mark flip-flop (CWFMP+), setting the write enable flip-flop (CWRTP+) and initiating tape motion (FWDCM+). The motion busy status is raised and the read block delay triggered to reset the read block flip-flop. A write oscillator delay is initiated and sustained for eight times the length of an inter-record gap delay to create a file mark gap of 3.7 inches. When the delay expires the

write strobe enable flip-flop is set and enables the file mark strobe WCFMS- to be generated. This strobe sets bit positions 02 and 03 of the NRZ register and triggers the write pulse delay. The inversion WCFMS+ sets the file strobe storage flip-flop and generates W7TFM- which sets bit positions 01 and 04 of the NRZ register. Signal WCFSS+ enables the write reset pulse to be generated four frame spaces later. This pulse WCWRP- resets the NRZregister and triggers WRTPL+ to produce the longitudinal parity character. The operation is terminated and tape motion halted in the same manner as that described for normal write operations.

Forward One Record/Forward One File

These are two separate operations illustrated in flow chart Figure 4-7 which are combined for description purposes due to their similarity. The operations are initiated by OCP'111x and OCP'121x respectively. In the forward one record operation the required MTT is selected (SELTx+), the PIL00- line is deactivated by CALLP+ and the erase head disabled by CRERS+. Forward motion is initiated by CFWDP+ which sets the forward flip-flop and resets the motion reverse history flip-flop. Signals MBSYS+, FWDCM+ and SYSRG+ are derived from forward flip-flop function MFWDF+ to establish the motion busy status, set the MTT in motion and trigger the read block delay (AUXCP+) to reset the read block flip-flop. The TCU reads the record but does not transfer data to the CP. Tranfers are prevented by RCDIP+ which is inhibited by READF+ which is not true. When the end of record gap RCEOR+ is detected tape motion is terminated in the normal manner.

In forward one file operations the TCU is initialised as for forward one record but with the search for file mark flip-flop set. The MTT is set in motion and the TCU reads the tape. Any interrecord gap detected without the file mark detected flip-flop set is ignored. Detection of the file mark sets the file mark detected flip-flop and RCFMD+ in conjunction with RCEOR+ generates RCEOP+ to terminate the operation in the normal manner.

Back Space One Record/Back Space One File

The back space one record and back space one file operations shown in flow chart Figure 4-8 are initiated by OCP'151x and OCP'161x commands respectively. The required MTT is selected and reverse motion is initiated by CREVP-. The remainder of the initialisation, and the actions which precede detection of RCEOR+ and RCFMD+ are as described under forward one record/forward one file.

When the required end of record gap or end of record gap and file mark are detected signal RCEOP+ is generated. Signal RCEOP+ triggers the reverse extention, REVEX- and generates MREST+ to halt tape motion. REVEX- sustains MBSYS+ for a further 8 milli-seconds at the end of which the end of motion interrupt is generated. If the load point, STLDP- is detected before the required end of record gap or file mark is found the operation is terminated by STLDP- which resets the reverse motion flip-flop.

Tape Rewind

The rewind operation shown in flow chart, Figure 4-9 is initiated by an OCP'141x command. On receipt of the command the TCU selects the required MTT and initiates the rewind by setting the rewind flip-flop (CRWDP+) and the erase flip-flop (CRERS+). RWDCM+ becomes true, sets the MTT in motion, sets the rewind status flip-flop, triggers AUXCP+ and enables triggering of the rewind extension. The reset level of the rewind flip-flop, RWDCM- raises the motion busy status MBSYS+. The 120 milli-second rewind extension is triggered by AUXCP+. When the rewind extension has expired the output of B37B resets the rewind flip-flop. MBSYS+ becomes not true to generate EMINT+ and the TCU becomes available to process commands for another associated MTT.

If the load point marker is detected before the rewind extension has expired STLDP-resets the rewind flip-flop. This terminates the operation and both the TCU and MTT become available to process further commands.

Table 4-2 Signal Mnemonics and Functions

Address and Control Logic

SIGNAL	LBD No.	SOURCE	DEFINITION
AOCP0	E010	K6	OCP and address
AOCP1	E010	K2	OCP and address
A1XXX	E010	B9	Address bit 7 = one
A3V7X	E010	F6	Address 3 or 7
AXxXX	E010	H1-H10	Decoded function bits
CALLP	E010	K7	Any OCP
CEVPP	E011	A8	Even Parity OCP
CFWDP	E011	D4	Forward OCP
CRERS	E011	E6	Reset erase
CREVP	E011	A7	Reverse OCP
CRINT	E011	C1	Control ready interrupt
CRTEP	E011	A5	Read OCP
CRWDP	E011	B7	Rewind OCP
CSFMP	E011	A2	Search file OCP
CW3BY	E011	A11	Write three binary OCP
CWDAP	E011	C2	Write data OCP
CWFMP	E011	D10	Write file mark OCP
CWRDP	E011	D9	Write or read data OCP
CWRTP	E011	C3	Write OCP
MTADD	E010	B3	Magnetic tape address
MTINT	E011 E011	G2 J8	Magnetic tape interrupt
MTMSK	E011	K9	Magnetic tape mask
S2CPW	E010	K1	Set two-characters-per-word OCP
XXXXx	E010	E2-E5	MTT selection
		Motion Control Logic	
ABUSY	E013	F3	MTTA busy
AUXCP	E013	G8	Auxiliary control pulse
BBUSY	E013	G3	MTTB busy
BSYEX	E013	F1	Busy extension

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
CBUSY	E013	J3	MTTC busy
DBUSY	E013	K3	MTTD busy
EOTSF	E013	E9	End of tape storage
EMINT	E013	D1	End of motion interrupt
FWDCM	E013	C7	Forward command
FWREX	E013	J10	Forward write extension
MBSYS	E013	C4	Motion busy status
MFWDF	E013	A7	Motion forward flip-flop
MHOLD	E013	F6	Motion hold
MREST	E013	K10	Motion reset
MREVF	E013	A10	Motion reverse flip-flop
MREVH	E013	A5	Motion reverse history
RBLKF	E013	K8	Read block flip-flop
RDBLK	E013	K9	Read block
REVCM	E013	C9	Reverse command
REVEX	E013	G10	Reverse extension
RWDCM	E013	G5	Rewind command
SYSRG	E013	C8	System read gate
		MTT Selection Logic	
AADDC	E014	H1	MTTA address compare
BADDC	E015	H1	MTTB address compare
CADDC	E016	H1	MTTC address compare
DADDC	E017	H1	MTTD address compare
SAHIC	E014	J6	Select MTTA high channels
SALOC	E014	J7	Select MTTA low channels
SBHIC	E015	J7	Select MTTB high channels
SBLOC	E015	J8	Select MTTB low channels
SBUSY	E014 E015 E016 E017	F9 F9 F9 F9	Selected MTT busy
SCHIC	E016	J6	Select MTTC high channels

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
SCHxH	E014 E015 E016 E017	A1-A8 A1-A8 A1-A8 A1-A8	Selected channel 1 through 9 high
SCHxL	E014 E015 E016 E017	D1-D8 D1-D8 D1-D8 D1-D8	Selected channel 1 through 9 low
SCLOC	E016	J8	Select MTTC low channels
SDHIC	E017	J7	Select MTTD high channels
SDLOC	E017	J8	Select MTTD low channels
SECHO	E014 E015 E016 E017	A10 A10 A10 A10	Selected echo
SELTA	E014	L2	Select MTTA
SELTB	E015	L1	Select MTTB
SELTC	E016	L1	Select MTTC
SELTD	E017	L1	Select MTTD
SLNHE	E014 E015 E016 E017	A9 A9 A9 A9	Selected low not high error
SREDY	E014 E015 E016 E017	G7 G7 G7 G7	Select ready (drive operational)
STEOT	E014 E015 E016 E017	D9 D9 D9 D9	Selected end of tape
STLOD	E014 E015 E016 E017	F8 F8 F8 F8	Selected low density
STLDP	E014 E015 E016 E017	D10 D10 D10 D10	Selected load point

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
STWAT	E014 E015 E016 E017	F10 F10 F10 F10	Selected write alignment test
SWPER	E014 E015 E016 E017	F7 F7 F7 F7	Selected write permit
TAxHI	E014	MTTA	MTTA channels 1 through 9 high output
TAxLO	E014	MTTA	MTTA channels 1 through 9 low output
TAADx	E014	MTTA	MTTA address 0 through 7
TAADC	E014	MTTA	MTTA address common
TABOT	E014	MTTA	MTTA beginning of tape
TADYC	E014	MTTA	MTTA density common
TAEOT	E014	MTTA	MTTA end of tape
TAHID	E014	MTTA	MTTA high density
TAHIP	E014	MTTA	MTTA head in position
TAHRT	E014	MTTA	MTTA HIP return
TALNH	E014	MTTA	MTTA low not high
TAPER	E014	MTTA	MTTA permit
TAPRT	E014	MTTA	MTTA permit return
TAWAT	E014	MTTA	MTTA write alignment test
TAWPE	E014	MTTA	MTTA write pulse echo
TBxHI	E015	MTTB	MTTB channels 1 through 9 high output
TBxLO	E015	MTTB	MTTB channels 1 through 9 low output
TBADx	E015	MTTB	MTTB address 0 through 7
TBADC	E015	MTTB	MTTB address common
TBBOT	E015	MTTB	MTTB beginning of tape
TBDYC	E015	MTTB	MTTB density common
TBEOT	E015	MTTB	MTTB end of tape
TBHID	E015	MTTB	MTTB high density

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
TBHIP	E015	MTTB	MTTB head in position
TBHRT	E015	MTTB	MTTB HIP return
TBLNH	E015	MTTB	MTTB low not high
TBPER	E015	MTTB	MTTB permit
TBPRT	E015	MTTB	MTTB permit return
TBWAT	E015	MTTB	MTTB write alignment test
TBWPE	E015	MTTB	MTTB write pulse echo
TCxHI	E016	MTTC	MTTC channels 1 through 9 high output
TCxLO	E016	MTTC	MTTC channels 1 though 9 low output
TCADx	E016	MTTC	MTTC address 0 through 7
TCADC	E016	MTTC	MTTC address common
TCBOT	E016	MTTC	MTTC beginning of tape
TCDYC	E016	MTTC	MTTC density common
TCEOT	E016	MTTC	MTTC end of tape
TCHID	E016	MTTC	MTTC high density
TCHID	E016	MTTC	MTTC head in position
TCHRT	E016	MTTC	MTTC HIP return
TCLNH	E016	MTTC	MTTC low not high
TCPER	E016	MTTC	MTTC permit
TCPRT	E016	MTTC	MTTC permit return
TCWAT	E016	MTTC	MTTC write alignment test
TCWPE	E016	MTTC	MTTC write pulse echo
TDxHI	E017	MTTD	MTTD channels 1 through 9 high output
TDxLO	E017	MTTD	MTTD channels 1 through 9 low output
TDADx	E017	MTTD	MTTD address 0 through 7
TDADC	E017	MTTD	MTTD address common
TDBOT	E017	MTTD	MTTD beginning of tape
TDDYC	E017	MTTD	MTTD density common
TDEOT	E017	MTTD	MTTD end of tape

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
TDHID	E017	MTTD	MTTD high density
TDHIP	E017	MTTD	MTTD head in position
TDHRT	E017	MTTD	MTTD HIP return
TDLNH	E017	MTTD	MTTD low not high
TDPER	E017	MTTD	MTTD permit
TDPRT	E017	MTTD	MTTD permit return
TDWAT	E017	MTTD	MTTD write alignment test
TDWPE	E017	MTTD	MTTD write pulse echo
		MTT Driver Logic	
ERASA	E018	D3	MTTA erase
ERASB	E019	D3	MTTB erase
ERASC	E020	D3	MTTC erase
ERASD	E021	D3	MTTD erase
SARWD	E018	D9	Select MTTA rewind
SBRWD	E019	D9	Select MTTB rewind
SCRWD	E020	D9	Select MTTC rewind
SDRWD	E021	D9	Select MTTD rewind
SRWDS	E018 E019 E020 E021	E8 E8 E8 E8	Selected rewind status
TA15V	E018	MTTA	MTTA +15 volts
TAERG	E018	E3	MTTA erase gate
TAFWD	E018	J3	MTTA forward
TARGD	E018	J9	MTTA read gate
TAREV	E018	J4	MTTA reverse
TARRS	E018	J1	MTTA read reset
TARWD	E018	D7	MTTA rewind
TAWCx	E018	G1-G6 J6-J8	MTTA write channel 1 through 9
TAWRP	E018	J10	MTTA write pulse
TAWTG	E018	J2	MTTA write gate

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
TB15V	E019	MTTB	MTTB +15 volts
TBERG	E019	E3	MTTB erase gate
TBFWD	E019	J3	MTTB forward
TBRDG	E019	J9	MTTB read gate
TBREV	E019	J4	MTTB reverse
TBRRS	E019	J1	MTTB read reset
TBRWD	E019	D7	MTTB rewind
TBWCx	E019	G1-G6 J6-J8	MTTB write channels 1 through 9
TBWRP	E019	J10	MTTB write pulse
TBWTG	E019	J2	MTTB write gate
TC15V	E020	MTTC	MTTC +15 volts
TCERG	E020	E3	MTTC erase gate
TCFWD	E020	J3	MTTC forward
TCRDG	E020	J9	MTTC read gate
TCREV	E020	J4	MTTC reverse
TCRRS	E020	J1	MTTC read reset
TCRWD	E020	D7	MTTC rewind
TCWCx	E020	G1-G6 J6-J8	MTTC write channels 1 through 9
TCWRP	E020	J10	MTTC write pulse
TCWTG	E020	J2	MTTC write gate
TD15V	E021	MTTD	MTTD +15 volts
TDERG	E021	E3	MTTD erase gate
TDFWD	E021	J3	MTTD forward
TDRDG	E021	J9	MTTD read gate
TDREV	E021	J4	MTTD reverse
TDRRS	E021	J1	MTTD read reset
TDRWD	E021	D7	MTTD rewind
TDWCx	E021	G1-G6 J6-J8	MTTD write channels 1 through 9
TDWRP	E021	J10	MTTD write pulse
TDWTG	E021	J2	MTTD write gate

Table 4-2 Signal Mnemonics and Functions (Continued)

Read Control

SIGNAL	LBD No.	SOURCE	DEFINITION
COLLD	E024	E6	Collection delay
COLLF	E024	C6	Collection flip-flop
EXSTP	E023	L4	External stop
LNHEF	E023	K2	Low not high error flip-flop
NTRES	E024	F6	No trespass
ROL12	E022	B1	Read octal 12
RCDIP	E023	L1	Read control drop in pulse
RCEOF	E023	F10	Read control end of file
RCEOP	E023	K9, K10	Read control end of operation
RCEOR	E024	L4	Read control end of record
RCFMD	E023	C7	Read control file mark detected
RCPEF	E023	K7	Read control parity error flip-flop
RCRWL	E023	K5	Read control read or write level
RCSFM	E023	H10	Read control search file mark
RDDB2	E022	E1	Read data decoded bit 2
RDDB4	E022	E3	Read data decoded bit 4
RDRES	E024	F3	MTT read buffer reset
READF	E023	J4	Read flip-flop
RGAPD	E024	L2	Gap detected pulse
RGCEN	E024	G2	Gap counter enable
RGCSx	E024	D9-L9	Gap counter stage 1 through 5
RGDET	E024	A4	Gap detected flip-flop
RGECR	E024	B9	Gap counter enable clock
RGSSY	E024	E1	Gap counter set synchronized
RSDLY	E024	A1	Read strobe delay
RSPEF	E022 E023 E024 E025	K4 H4, H5 G4 L7	Set parity error flip-flop
RSTRB	E024	B1	Read strobe
STRBx	E022	C4-C10	Selected read bits 1 through 7

Table 4-2 Signal Mnemonics and Functions (Continued)

Write Control

SIGNAL	LBD No.	SOURCE	DEFINITION
MWELF	E026	J5	Write enable flip-flop
MWLDP	E026	H9	Write at load point
MWSEN	E026	H9	Write strobe enable
NINET	E025	B7	Nine track (not used)
W7TFM	E025	C4	Write seven track file mark
WCCLK	E025	F4 K5	Write control clock
WCFMS	E025	A5	Write control file mark strobe
WCFRK	E025	K4	Write control frame rate clock
WCFSS	F025	D5	Write control file strobe storage
WCNWS	E025	A3	Write control normal write strobe
WCRCS	E025	F7	Write cyclic redundancy character strobe
WCWFM	E025	H10	Write control write file mark
WCWRP	E025	F10	Write control write reset pulse
WHICK	E025	A1	Write high clock
WLOCK	E025	E1	Write low clock
WLDPG	E026	L1	Write load point gate
WRITE	E026	L5	Write
WRTPL	E025	K8	Write pulse
WOSDT	E026	J3	Write oscillator delay trigger
		Buffer and Control	
B2CPW	E027	B2	Buffer two-characters-per-word
BCECx	E027	F1, H1 K1	Buffer control enable character 1 through 3
BCH3T	E027	D1	Buffer character three time
BCHDx	E027	F3, H3, K3	Buffer character distributor 1 through 3
BCLCT	E027	D2	Buffer control last character time
BCRDY	E027	E9	Buffer control ready
BCRES	E027	K6	Buffer control reset
BCSCx	E027	K8-K10	Buffer control strobe character 1 through 3

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
BEINB	E027	C5	Buffer enable input bus
BTTOE	E027	K7	Buffer transfer output bus enable
BWDBx	E030	J1-J10	Buffer write data bits 1 through 6
BXFCF	E027	G8	Buffer transfer control flip-flop
BXFER	E027	G5	Buffer transfer
CEVEN	E031	C9	Even parity
LCT2C	E027	C1	Last character time, two characters
RIBxx	E028	C1-C7 E1-E7 K1-K7	Rank one, bits 1 through 16
R2Bxx	E029	B2-B9 E2-E9 J2-J9	Rank two, bits 1 through 18
RESR1	E027	H5 F10	Reset rank one
RRLAO	E027	B10	Reset ready line and address
RRLAX	E027	B9	Reset ready line and address
S1Bxx	E028	B1-B8 D1-D8 J1-J8	Set rank one, bits one through 16
WDATx	E031	K1-K10	Write data tracks 1 through 7
WZERO	E031	F2	Write zero
		DMA/DMC Subchannel	
ACKAX	E012	DMA	Acknowledge from DMA
CHANB	E012	G3	Autoswitch subchannel B
CHENX	E012	DMA	Channel enable from DMA
CHSLI	E012	C7	Channel select
CHSLX	E012	DMA	Channel select from DMA
DACKR	E012	A10	Data acknowledge ready
DALXX	E012	DMC	Device address lines from DMC
DAUTO	E012	G9	Autoswitch mode flip-flop
DERLF	E012	G7	End or range flip-flop
DERLX	E012	B5	End of range

Table 4-2 Signal Mnemonics and Functions (Continued)

SIGNAL	LBD No.	SOURCE	DEFINITION
DILAX	E012	K2, K5	Data interrupt lines to DMA
DILXX	E012	K2, K4	Data interrupt lines to DMC
DMCAD	E012	B4	DMC address
DMCMF	E012	E1	DMC mode flip-flop
ENDXM	E012	K7	End of transmission
EXSPF	E012	G3	External stop flip-flop
REDMC	E012	A3	Reset DMC OCP
RRLAO	E012	C9	Reset ready line and address
SDMCA	E012	A2	Set DMC auto OCP
SDMCN	E012	A1	Set DMC normal OCP

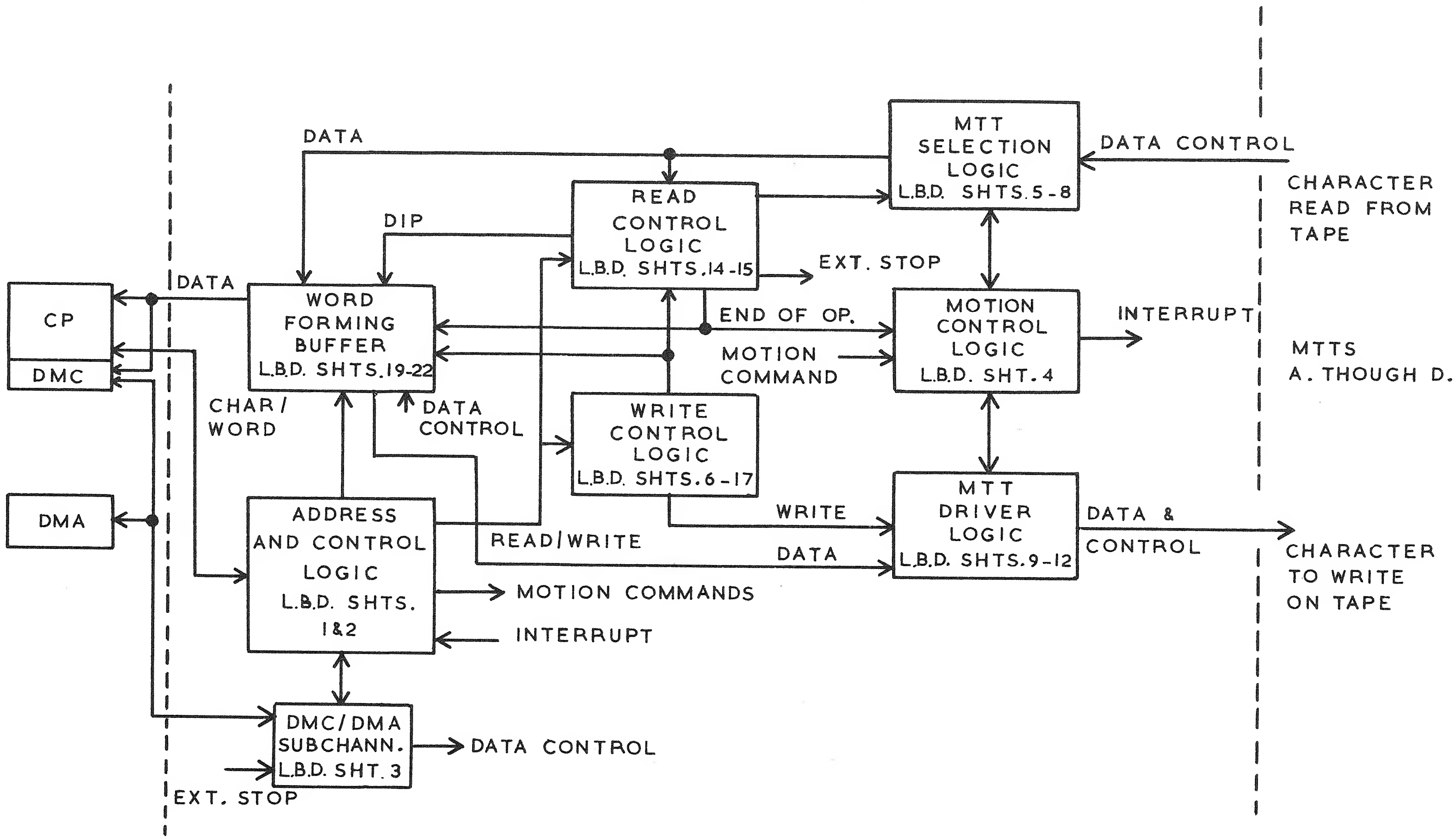


Figure 4-1 Tape Control Unit - Block Diagram

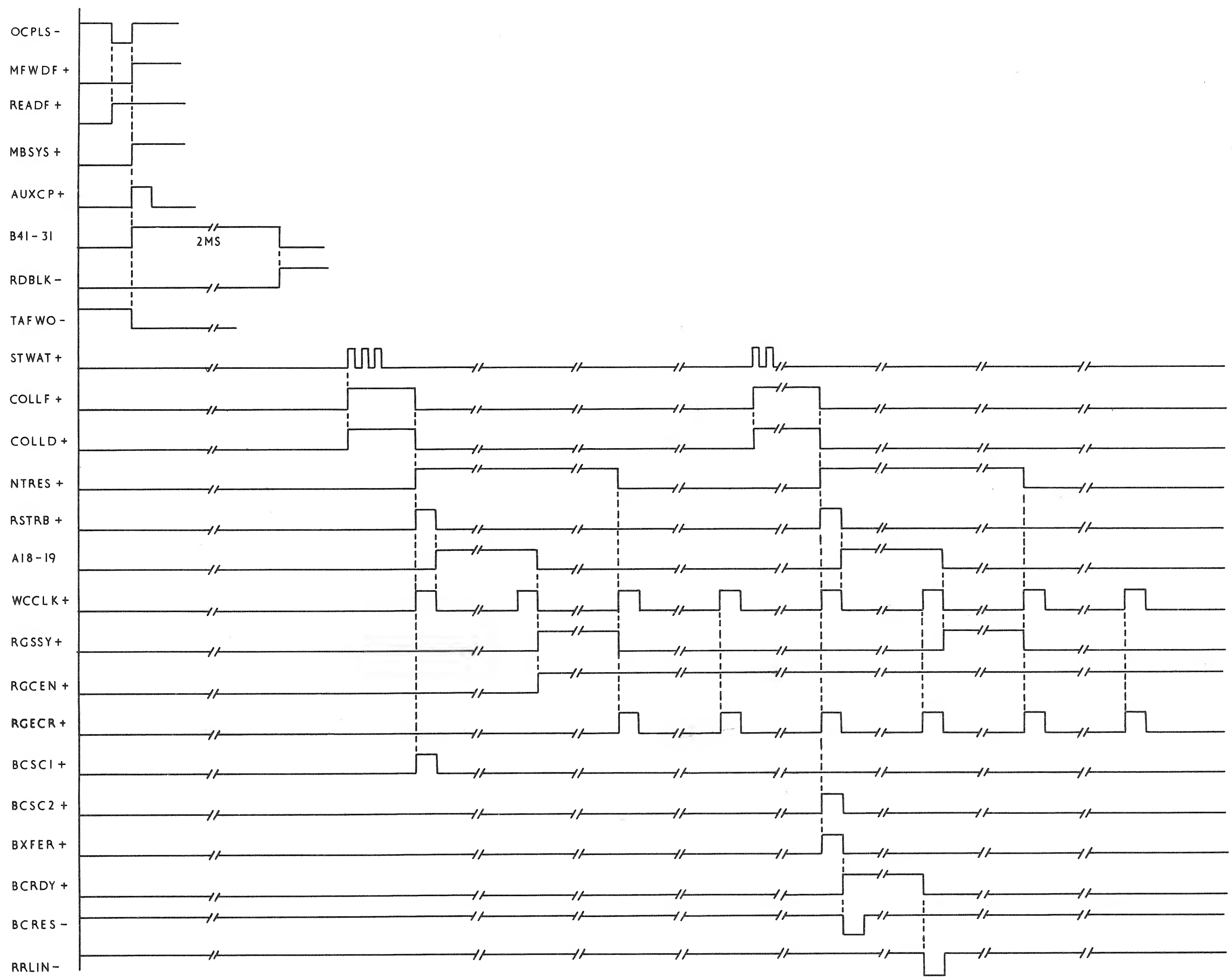


Figure 4-2 Read BCD/Binary Two Characters Per Word

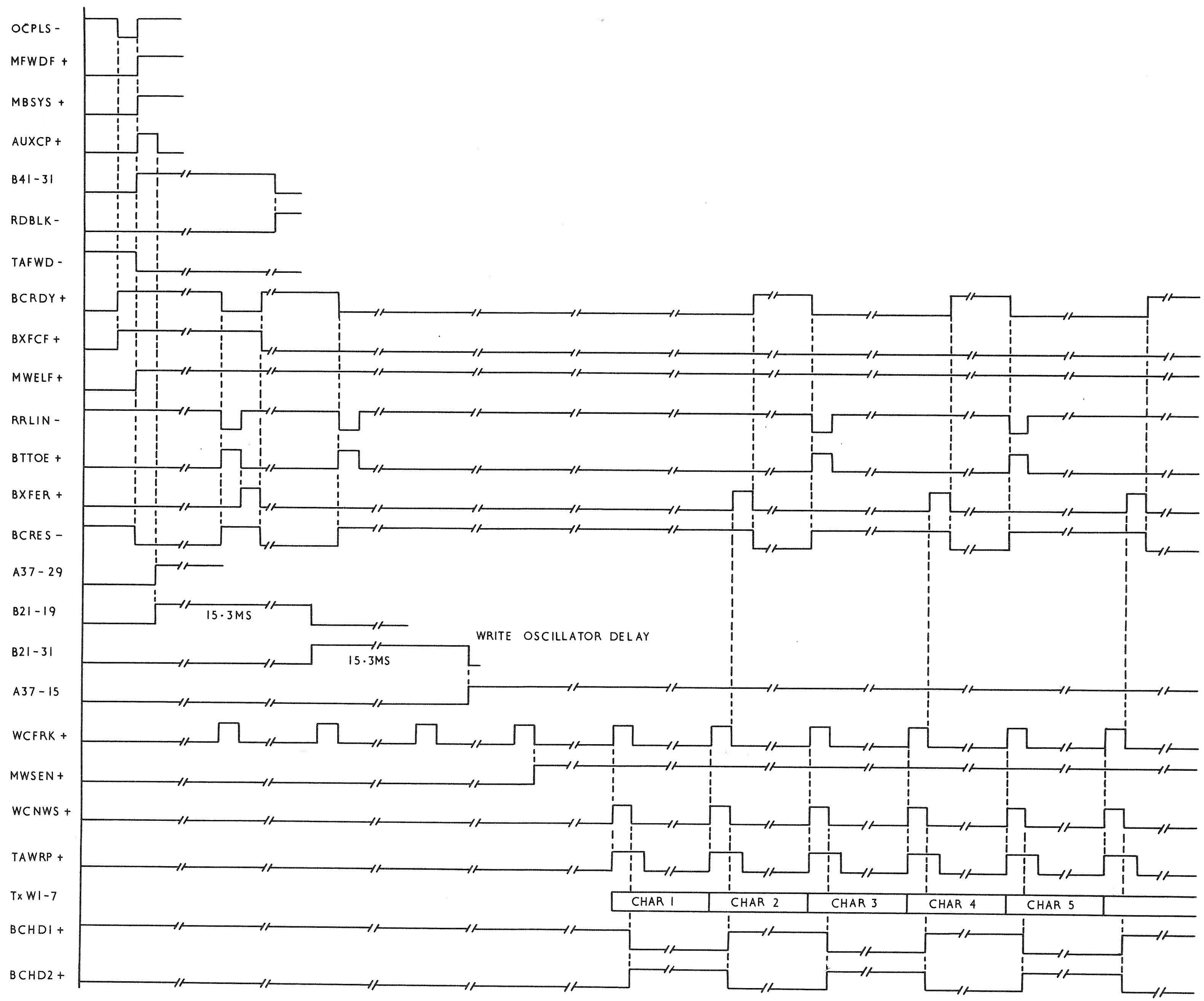


Figure 4-3 Write BCD/Binary Two Characters Per Word

Read One BCD/Binary Record, 2 Char/Word

(Initiated by OCP'001x or OCP'011x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+A ADB14-A	E010-E10 E010-J5	Enable octal/binary converter Enable generate AOCP0+
AOCP0+	E010-K6	OCPLS+ MBSYS- MTADD+ A1XXX-	E010-K7 E011-A5 E027-A2	Generate CALLP+ Enable Generate CRTEP- Clock B2CPW flip-flop
CALLP+	E010-K7	AOCP0+	E013-A3 E014-H3 E015-H3 E016-H3 E017-H3 E023-F10	Reset B45A and B45B flip-flop Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop Reset RCEOF flip-flop
S2CPW+	E010-K1	AX0XX- AX1XX-	E027-A2	Set level for B2CPW flip-flop
CEVPP-	E011-A8	AX0XX- AOCP0+	E031-D9	Set CEVEN flip-flop if BCD mode
B2CPW+	E027-B2	S2CPW+ AOCP0+	E027-C2	Generate BCLCT+
CRTEP-	E011-A5	AX0XX- AX1XX- AOCP0+	E011-D4 E011-E6 E011-B7 E023-J4 E027-J6	Generate CFWDP+ Generate CRERS+ Generate CWRDP+ Set READF flip-flop Generate BCRES-
CFWDP+	E011-D4	CRTEP-	E013-A5 E013-A7 E013-B4	Reset MREVH flip-flop Set MFWDF flip-flop Enable set MHOLD flip-flop
CRERS+	E011-F6	CRTEP-	E018-A4 E019-A4 E020-A4 E021-A4	Enable reset ERASA flip-flop Enable reset ERASB flip-flop Enable reset ERASC flip-flop Enable reset ERASD flip-flop
CWRDP+	E011-D9	CRTEP-	E027-E2 E022-F10	Set character distributor to 4_8 Reset longitudinal parity checker
READF+	E023-J4	CRTEP-	E023-J1 E027-A5 E027-C5 E027-C5 E027-C9 E027-F9	Enable generate RCDIP+ Enable generate BEINB+ Enable generate RESR1- Enable buffer character distributor clock Enable generate BXFER+ Enable generate RSPEF-
BCRES-	E027-K6	CRTEP-	E028-A10	Reset R1B
MREVH-	E013-A5	CFWDP+	E013-A5	Set MHOLD flip-flop

Read One BCD/Binary Record, 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
MFWDF+	E013-A7	CFWDP+	E013-C4 E013-B7 E013-B7	Generate MBSYS+ Enable generate FWDCM+ Enable generate SYSRG+
MBSYS+	E013-C4	MFWDF+	E010-F4 E011-F6 E013-B3 E023-H10	Inhibit generate AOCP0+ AOCP1 Motion busy status for SKS'011x Set level for B45B flip-flop Reset RCSFM flip-flop on TE
FWDCM+	E013-C7	MFWDF+ MHOLD- SWPER- MWELF+	E018-H3 E019-H3 E020-H3 E021-H3	Enable generate TAFWD- Enable generate TBFWD- Enable generate TCFWD- Enable generate TDFWD-
SYSRG+	E013-C8	MFWDF+ MHOLD- SWPER- MWELF+	E013-D8 E018-H9 E019-H9 E020-H9 E021-H9	Generate AUXCP+ Enable generate TARDG- Enable generate TBRDG- Enable generate TCRDG- Enable generate TDRDG-
AUXCP+	E013-G8	SYSRG+	E013-H7 E013-E10	Reset RBLKF flip-flop in 2 milli-seconds Reset EOTSF flip-flop
ABUSY+ BBUSY+ CBUSY+ DBUSY+	E013-F3 E013-G3 E013-J3 E013-K3	SELTA+ B45-5 * SELTB+ B45-5 * SELTC+ B45-5 * SELTD+ B45-5 *	E014-E9 E015-E9 E016-E9 E017-E9	Enable generate SBUSY- at TE of MBSYS+
STWAT-	E014-F10 E015-F10 E016-F10 E017-F10	TAWAT+ SELTA+A * TBWAT+ SELTB+A * TCWAT+ SELTC+A * TDWAT+ SELTD+A *	E024- E024-	Enable set COLLF flip-flop Enable generate RSPEF-
COLLF+	E024-C6	STWAT+ NTRES- RDBLK-	E024-D6	Trigger collection delay
COLLD+	E024-E6	COLLF+	E024-F6	Set NTRES flip-flop
NTRES+	E024-F6	COLLD+	E024-A1	Trigger read strobe delay
RSDLY-	E024-A1	NTRES+	E024-B1	Generate RSTRB+
RSTRB+	E024-B1	RSDLY-	E024-D1 E022-F8 E023-B8 E023-A10 E023-G5	Set A18E flip-flop on TE Clock longitudinal parity checker Reset A13C flip-flop on TE Enable file mark detector Enable set RCPEF flip-flop on lateral parity error

*Dependent upon which MTT is selected

Read One BCD/Binary Record, 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
RSTRB+	E024-B1	RSDLY-	E023-J1 E023-K2 E024-C4	Enable generate RCDIP+ Reset LNHEF flip-flop Enable set A18B if gap detected
STRB1-7	E022-C4-C10	SCHxH- SCHxL-	E022-F1-F10 E022-A1-A3 E023-A1-A10 E028-A1-A8 C1-C4	Set level control for longitudinal parity checker Input for zero code restoration Inputs for lateral parity pyramid and file mark detector Inputs to R1B
BCEC1+	E027-H1	BCHD1+ NINET-	E027-J8	Enable generate BCSC1+
RCDIP+	E023-K1	READF+ RGDET- RSTRB+ MREVF-	E027-J8 E027-A6	Generate BCSC1+ Trigger A11A to generate BXFER+ and clock buffer character distributor
BCSC1+	E027-K8	BCEC1+ RCDIP+	E028-A9	Strobe first character into R1B
RGSSY+	E024-E1	A18-19 WCCLK+	E024-F6	Reset NTRES flip-flop on TE
RGSSY-	E024-E1	A18-19 WCCLK+	E024-F1 E024-F3 E024-B8	Set RGCEN flip-flop Generate RDRES+ Set gap counter to 37_8
RGCEN+	E024-G1	RGSSY-	E023-D8 E024-A9	Enable reset RCFMD flip-flop Enable generate RGECR+
RDRES+	E024-F3	RGSSY- RDBLK-	E018-H1 E019-H1 E020-H1 E021-H1	Enable generate TARRS- Enable generate TBRRS- Enable generate TCRRS- Enable generate TDRRS-
RGECR+	E024-B9	RGCEN+ WCCLK+	E024-C9	Gap counter enable
NOTE: Generate RSTRB+ with STWAT- and perform repetitive functions.				
BCEC2+	E027-K1	BCHD2+ NINET-	E027-J9	Enable generate BCSC2+
BCSC2+	E027-K9	BCEC2+ RCDIP+	E028-C9	Strobe second character into R1B
BXFER+	E027-G5	RCDIP+ BCLCT+	E027-E8 E027-G9 E029-A10	Set BCRDY flip-flop on TE Enable generate RSPEF- Enter R1B data into R2B
RESR1-	E027-F10	READF+ A11-19 BCLCT+	E027-J5	Generate BCRES-
BCRES-	E027-K6	RESR1-	E028-A9	Reset R1B

Read One BCD/Binary Record, 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
BCRDY+	E027-E9	BXFER+	E011-G5 E011-J8	Generate DRLIN- in response to SKS'001x and INA'101x Enable generate MTINT- if interrupt mask is set
DRLIN-	E011-L2 E011-J5	BCRDY+ AX0XX+ AX1XX+ or BCRDY+ AX0XX+ AX1XX-	CP	Device ready line
RRLIN+	E027-A9	RRLIN-	E027-B9	Enable generate RRLAX-
RRLAX-	E027-B9	RRLIN+ MTADD+	E027-E9	Reset BCRDY flip-flop
BEINB+	E027-C5	READF+ MTADD+	E029-A11	Gate R2B contents onto INB
Procedure repeated for remainder of record until no data gap is detected.				
RGAPD+	E024-L2	RGCS1+ RGCS2- RGCS3+ RGCS4- RGCS5- RGECR+	E024-A4 E027-C9	Set RGDET flip-flop on TE Enable generate BXFER+
STRB1-7	E022-C4-C10	SCHxH- SCHxL-	E022-F1-F10	Input to longitudinal parity checker
RCEOR+	E024-L4	RGCS1+ RGCS2- RGCS3+ RGCS4+ RGCS5+ RGECR+	E022-J4 E023-D10 E023-J10 E024-F2 E024-A4 E031-D9	Enable generate RSPEF- Enable set RCEOF flip-flop Enable generate RCEOP+ Reset RGCEN flip-flop Reset RGDET flip-flop Reset CEVEN flip-flop on TE
RSPEF-	E024-G4	RSTRB+ A18-7	E023-K7	Set RCPEF flip-flop if RSTRB+ is received before RCEOR+
RCEOP-	E023-K9	RCEOR+ RCSFM-	E013-K10	Generate MREST+
RCEOP+	E023-L10	RCEOR+ RCSFM-	E013-K8 E023-J4	Set RBLKF flip-flop Reset READF flip-flop
MREST+	E013-K10	RCEOP+	E013-A7	Reset MFWDF flip-flop
BSYEX+	E013-F1	MBSYS+ (TE)	E013-F2 E013-E7	Reset BUSY flip-flop after 8 milli-seconds Reset MHOLD flip-flop
EMINT+	E013-D1	B45-1 B45-8	E011-G2	Generate MTINT- on TE if interrupt mask set
MTINT-	E011-G2	EMINT+ MTMSK+	E011-K7	Activate PIL00-
CALLP+	E010-K7	AOCP0+ AOCP1+	E013-A3	Deactivate PIL00- with subsequent magnetic tape OCP

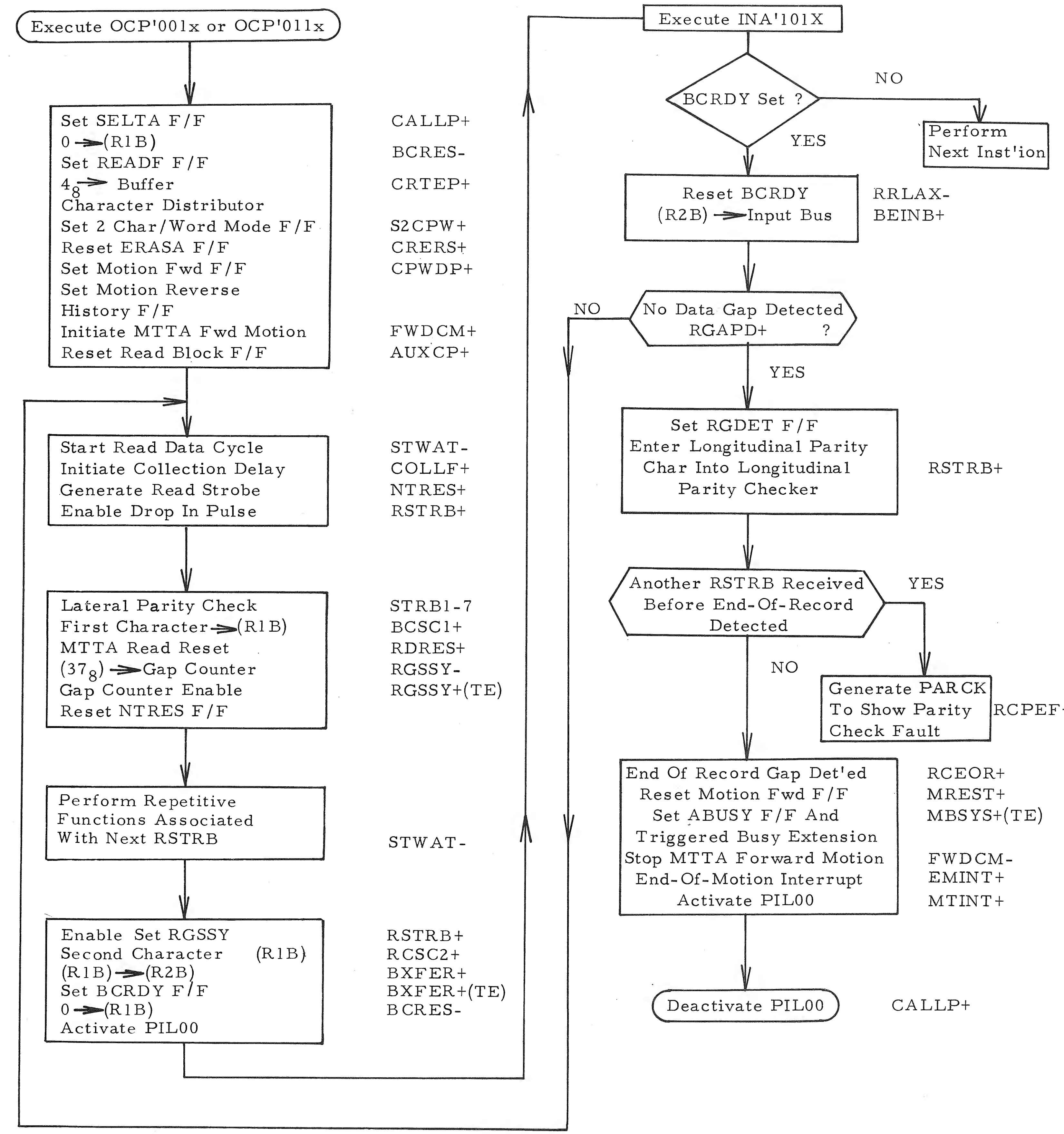


Figure 4-4 Read One BCD/Binary Record, 2 Characters Per Word - Flow Chart

Write One BCD/Binary Record 2 Char/Word

(Initiated by OCP'041x or OCP'051x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+A ADB14-A	E010-F10 E010-J5	Enable octal/binary converter Enable generate AOCP0+
AOCP0+	E010-K6	OCPLS+ MBSYS- MTADD+ A1XXX-	E010-K7 E011-A3 E027-A2	Generate CALLP+ Enable activate output A48-2 Clock B2CPW flip-flop
CALLP+	E010-K7	AOCP0+	E013-A3 E014-J3 E015-J3 E016-J3 E017-J3 E023-F10	Reset B45A and B45B flip-flops Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop Reset RCEOF flip-flop
S2CPW+	E010-K1	AX4XX- AX5XX-	E027-A2	Set level for B2CPW flip-flop
CEVPP	E011-A8	AX4XX- AOCP0+	E031-C9	Set CEVEN flip-flop if BCD mode
B2CPW+	E027-B2	S2CPW+ AOCP0+	E027-C2	Enable generate BCLCT+
CWDAP-	E011-C2	A48-2	E027-E8 E027-G7	Set BCRDY flip-flop to activate PIL00- Set BXFCF flip-flop
CWRDP-	E011-D9	A48-2	E027-E2 E022-F10	Set character distributor to 4_8 Reset longitudinal parity checker
CWRTP-	E011-C3	A48-2	E011-D4	Generate CFWDP+
CWRTP+	E011-C3	A48-2	E018-A3 E019-A3 E020-A3 E021-A3 E026-J5	Enable set ERASA flip-flop Enable set ERASB flip-flop Enable set ERASC flip-flop Enable set ERASD flip-flop Set MWELF flip-flop
BCRDY+	E027-E9	CWDAP-	E027-H6 E011-G5 E011-J8	Enable generate RESR1- Generate DRLIN- in response to SKS'001x and OTA'001x Enable generate MTINT if interrupt mask is set
BXFCF-	E027-G8	CWDAP-	E025-A3	Enable generate WCNWS+
BXFCF+	E027-G8	CWDAP-	E025-A7 E027-A6 E027-C7	Enable clock B44A flip-flop Enable trigger A11A Enable generate BXFER+
CFWDP+	E011-D4	CWRTP-	E013-A5 E013-A7 E013-A4	Reset MREVH flip-flop Set MFWDF flip-flop Enable set MHOLD flip-flop

Write One BCD/Binary Record 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
MWELF+	E026-J5	CWRTP-	E013-B7	Enable generate FWDCM+ and SYSRG+
			E013-J9	Enable trigger FWREX delay
			E023-G4	Enable generate RSPEF- on LNHEF+
			E024-B7	Enable generate RSPEF- on STWAT+
			E026-G9	Enable set MWLDP flip-flop
			E026-J3	Enable generate WOSDT-
			E027-H5	Generate RESR1- if BCRDY flip-flop set
			E027-A10	Enable generate RRLA0+
MWELF-	E026-J5	CWRTP-	E023-K5	Generate RCRWL+
			E026-K5	Generate WRITE+
RESR1-	E027-H5	MWELF+ BCRDY+	E027-J5	Generate BCRES- to reset R1B
MREVH+	E013-A5	CFWDP+	E013-A5	Set MHOLD flip-flop
MFWDF+	E013-A7	CFWDP+	E013-C4	Generate MBSYS+
			E013-C7	Generate FWDCM+
			E013-C7	Generate SYSRG+
MBSYS+	E013-C4	MFWDF+	E010-F4	Inhibit generate AOCP0- AOCP1-
			E011-F6	Motion busy for SKS'011x
			E013-B3	Set level for B45B flip-flop
			E023-G10	Reset RCSFM flip-flop on TE
FWDCM+	E013-C7	MFWDF+ MHOLD- SWPER+ MWELF-	E018-H3	Enable generate TAFWD-
			E019-H3	Enable generate TBFWD-
			E020-H3	Enable generate TCFWD-
			E021-H3	Enable generate TDFWD-
SYSRG+	E013-C8	MFWDF+ MHOLD- SWPER+ MWELF-	E013-E8	Generate AUXCP-
			E018-H9	Enable generate TARDG-
			E019-H9	Enable generate TBRDG-
			E020-H9	Enable generate TCRDG-
			E021-H9	Enable generate TDRDG-
WRITE+	E026-L5	MWELF+	E018-H2	Enable generate TAWTG-
			E019-H2	Enable generate TBWTG-
			E020-H2	Enable generate TCWTG-
			E021-H2	Enable generate TDWTG-
AUXCP+	E013-G8	SYSRG+	E013-H7	Reset RBLKF flip-flop in 2 milli-seconds
			E013-D10	Reset EOTSF flip-flop
			E026-J1	Enable generate WOSDT-

Write One BCD/Binary Record 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
WOSDT-	E026-J3	AUXCP+ MWELF+ MHOLD+ MWELF+	E026-A4	Set A37F flip-flop to trigger write oscillator delay which sets MWSEN flip-flop
RRLIN+	E027-A9	RRLIN-	E027-A9 E027-A10	Generate RRLAX- with MTADD+ Generate RRLAO with MTTAD+
RRLAX-	E027-B9	RRLIN+ MTADD+	E027-E9	Reset BCRDY flip-flop
RRLAO-	E027-B10	RRLIN+ MTADD+ MWELF+	E027-A7	Trigger A11A to generate BXFER+ Generate BTTOE+
A37-29	E026-C4	WOSDT-	E026-E4	Trigger write oscillator delay
BTTOE+	E027-K7	RRLAO-	E028-A9	Strobe OTB01 through OTB16 into R1B
BXFER+	E027-G5	A11-19 BCFCF+	E027-E9 E027-G8 E029-A10	Set BCRDY flip-flop Reset BXFCF flip-flop Strobe R1B into R2B
BCRDY+	E027-E9	BXFER+	E027-H6 E011-G5	Generate RESR1- to reset R1B Generate DRLIN- in response to SKS'001x and OTA'001x
The CP initiates a second data transfer into R1B but BXFER is not generated due to BXFCF+ being not true.				
STLOD-	E014-F8 E015-F8 E016-F8 E017-F8	TAHID- SELTA+A* TBHID- SELTB+A* TCHID- SELTC+A* TDHID- SELTD+A*	E025-A1 E025-C1	Enable WHICK clock † Disable WLOCK clock †
WHICK-	E025-A1	STLOD-	E025-A1	Generate WCCLK-
WCCLK-	E025-F4	WHICK-	E025-F2	Generate WCFRK+
B21-31	E026-G4	WOSDT-	E026-A6	Set A37D flip-flop
MWSEN+	E026-H8	A37-15 WCFRK+	E025-A3	Enable generate WCNWS-
BCHD1+	E027-F3	WCNWS-	E027-G1 E027-H3	Enable generate BCEC1+ Set level for BCHD2 flip-flop
BCEC1+	E027-H1	BCHD1+ NINET-	E030-B10	Strobe R2B bits 01 through 06 onto write bus

* Dependent upon which MTT is selected

† High density selected

Write One BCD/Binary Record 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
WCNWS-	E025-A3	BXFCF- WCWFM- WCFRK+ MWSEN+	E025-G7 E027-D4	Trigger WRTPL+ Clock character distributor
WCNWS+	E025-A3	WCNWS-	E031-H1	Strobe write bus data and lateral parity bit into NRZ register
WRTPL+	E025-K8	WCNWS-	E018-G10 E019-G10 E020-G10 E021-G10	Enable generate TAWRP+ Enable generate TBWRP+ Enable generate TCWRP+ Enable generate TDWRP+
WDAT1-7	E031-K1 -K10	WCNWS+ BWDB1+ through BWDB7+	E018-H5, F1-F7 E019-H5, F1-F7 E020-H5, F1-F7 E021-H5, F1-F7	Enable generate TAWC1- through TAWC7- Enable generate TBWC1- through TBWC7- Enable generate TCWC1- through TCWC7- Enable generate TDWC1- through TDWC7-
BCHD2+	E027-H3	WCNWS- BCHD1+	E027-J1 E027-C2	Enable generate BCEC2+ Generate BCLCT+
BCEC2+	E027-L1	BCHD2+ NINET-	E030-D10	Strobe R2B bits 07 through 12 onto write bus
WCNWS-	E025-A3	BXFCF- WCWFM- WCRFK+ MWSEN+	E025-G7 E027-D4 E027-E5	Trigger WRTPL+ Clock character distributor Enable generate BXFER+
WCNWS+	E025-A3	WCNWS-	E031-H1	Strobe write bus data and lateral parity bit into NRZ register
WRTPL+	E025-K8	WCNWS-	E018-G10 E019-G10 E020-G10 E021-G10	Enable generate TAWRP+ Enable generate TBWRP+ Enable generate TCWRP+ Enable generate TDWRP+
WDAT1 -7	E031-K1 -K10	WCNWS+ BWDB1+ through BWDB7+	E018-H5, F1-F7 E019-H5, F1-F7 E020-H5, F1-F7 E021-H5, F1-F7	Enable generate TAWC1- through TAWC7- Enable generate TBWC1- through TBWC7- Enable generate TCWC1- TCWC7- Enable generate TDWC1- through TDWC7-
BCLCT+	E027-D2	BCHD2+ B2CPW+	E027-F3 E027-F5	Set level for BCHD1 flip-flop Generate BXFER+
BXFER+	E027-G5	BCLCT+ WCNWS-	E027-E9 E029-A10	Set BCRDY flip-flop Strobe R1B into R2B

Write One BCD/Binary Record 2 Char/Word (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
BCRDY+	E027-E9	BXFER+	E027-H6 E011-G5	Generate RESR1- to reset R1B Generate DRLIN- in response to SKS'001x and OTA'001x
Continue writing until the last character in the record is written. Read after write logic checks lateral parity on each character.				
BXFCF+	E027-G8	BCRDY+ MWSEN+ BXFER+	E025-A8	Enable generate WCWRP- on fourth WCFRK+
WCWRP-	E025-F10	B44-6 B44-8 B44-31 B46-2 MWSEN+	E025-G7 E031-H10	Trigger WRTPL+ Reset NRZ register to generate longitudinal parity character
WCWRP+	E025-F10	WCWRP-	E025-H10 E025-C5 E026-G8	Reset WCWFM flip-flop on TE Reset WCFSS flip-flop on TE Reset MWSEN flip-flop on TE
Refer to read one BCD/Binary record 2 char/word analysis for events prior to detection of RGAPD+, ignoring read data transfers to CP.				
RGAPD+	E024-L2	RGCS1+ RGCS2- RGCS3+ RGCS4- RGCS5- RGECR+	E024-A4	Set RGDET flip-flop on TE
RCEOR+	E024-L4	RGCS1+ RGCS2- RGCS3+ RGCS4+ RGCS5+ RGECR+	E023-J10 E024-A4 E024-F2 E024-E4 E031-D9	Generate RCEOP- Reset RGDET flip-flop on TE Reset RGCEN flip-flop on TE Reset A18B flip-flop on TE Reset CEVEN flip-flop on TE
RCEOP-	E023-K9	RCEOR+ RCSFM-	E013-K10 E027-E9 E027-D10 E027-F8	Generate MREST Reset BCRDY flip-flop Generate RESR1- Reset BXFCF flip-flop
RCEOP+	E023-K10	RCEOP-	E013-G9 E013-K8	Trigger FWREX- Set RBLKF flip-flop
FWREX-	E013-J10	RCEOP+ MWELF+	E013-K10	Continue generation of MREST+
MREST+	E013-K10	RCEOP+ FWREX-	E013-A7 E026-J5	Reset MFWDF flip-flop Reset MWELF flip-flop
BSYEX+	E013-F1	MBSYS+ (TE)	E013-F2 E013-F6	Reset BUSY flip-flop after 8 milli-seconds Reset MHOLD flip-flop
EMINT+	E013-D1	B45-1 B45-8	E011-G2	Generate MTINT- on TE if interrupt mask set
MTINT-	E011-G2	EMINT+ MTMSK+	E011-K7	Activate PIL00-
CALLP+	E011-K7	AOCP0+ AOCP1+	E013-A3	Reset B45A and B45B to deactivate PIL00 on subsequent OCP

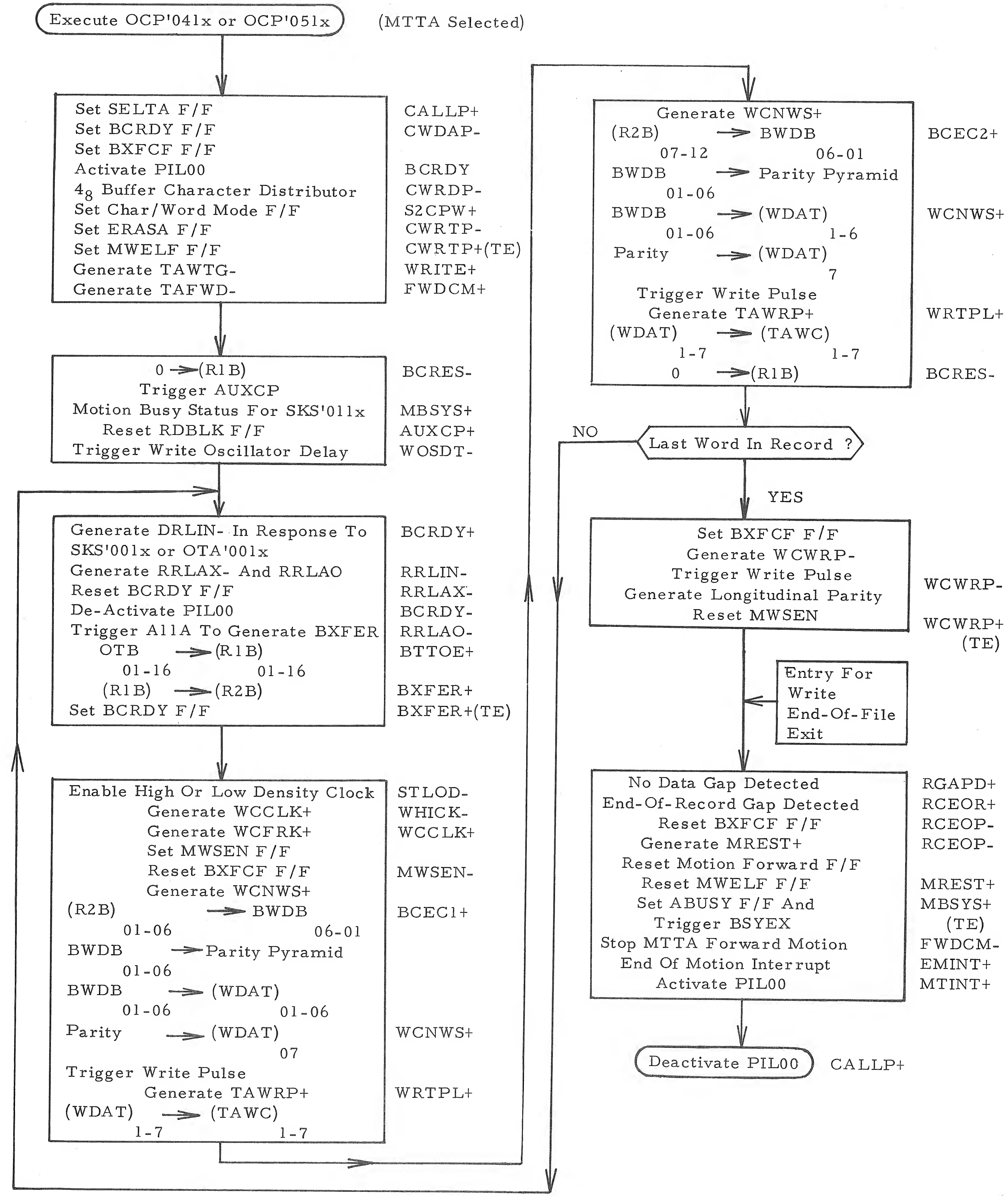


Figure 4-5 Write One BCD/Binary Record, 2 Characters Per Word - Flow Chart

Write End of File

(Initiated by OCP'061x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+A ADB14-A	E010-E10 E010-J5	Enable octal/binary converter Enable generate AOCP0+
AOCP0+	E010-K6	OCPLS+ MBSYS- MTADD+ A1XXX-	E010-K7 E011-D10	Generate CALLP+ Enable generate CWFMP-
CALLP+	E010-K7	AOCP0+	E013-A3 E014-J3 E015-J3 E016-J3 E017-J3 E023-F10	Reset B45A and B45B flip-flops Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop Reset RCEOF flip-flop
CWFMP	E011-D10	AX6XX+ AOCP0+	E011-C3 E025-H10	Generate CWRTP- Set WCWFM flip-flop
CWRTP-	E011-C3	CWFMP-	E011-D4	Generate CFWDP+
CWRTP+	E011-C3	CWFMP-	E018-A3 E019-A3 E020-A3 E021-A3 E026-J5	Enable set ERASA flip-flop Enable set ERASB flip-flop Enable set ERASC flip-flop Enable set ERASD flip-flop Set MWELF flip-flop with TE
CFWDP+	E011-D4	CWRTP-	E013-A5 E013-A7 E013-A5	Reset MREVH flip-flop Set MFWDF flip-flop Enable set MHOLD flip-flop
MFWDF+	E013-A7	CFWDP+	E013-C4 E013-C7 E013-C7	Generate MBSYS+ Generate FWDCM+ Generate SYSRG+
MYSYS+	E013-C4	MFWDF+	E010-F4 E011-F6 E013-B3 E023-G10	Inhibit generate AOCP0- AOCP1- Motion busy status for SKS'011x Set motion busy extension flip-flop Reset RCSFM flip-flop on TE
FWDCM+	E013-C7	MFWDF+ MHOLD- SWPER+ MWELF-	E018-H3 E019-H3 E020-H3 E021-H3	Enable generate TAFWD- Enable generate TBFWD- Enable generate TCFWD- Enable generate TDFWD-
SYSRG+	E013-C8	MFWDF+ MHOLD- SWPER+ MWELF-	E013-E8 E018-H9 E019-H9 E020-H9 E021-H9	Generate AUXCP+ Enable generate TARDG- Enable generate TBRDG- Enable generate TCRDG- Enable generate TDRDG-

Write End of File (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
WOSDT-	E026-J3	AUXCP+ MWELF+ MHOLD+ MWELF+	E026-A4	Set A37F flip-flop to generate gap
A37-29	E026-C4	WOSDT-	E026-E4	Trigger write oscillator delay
WCWFM+	E025-H10	CWFMP-	E025-A5 E026-A8	Enable generate WCFMS+ Enable set A37D flip-flop after eighth wrote oscillator delay pulse
A37-15	E026-E8	MWLDP- WCWFM- MWSEN- B38-14	E026-G8	Enable set MWSEN flip-flop
WCFMS+	E025-B5	WCFSS- WCWFM- WCFRK+ MWSEN+	E025-C5 E025-C4 E025-G7 E031-H3	Set WCFSS flip-flop Generate W7TFM- Trigger WRTPL+ Set WDAT2 and WDAT3 flip-flops
W7TFM-	E025-C4	WCFMS+	E031-Hl	Set WDATl and WDAT4 flip-flops
B43-18	E025-A10	WCFSS+ WCWFM+ WCFRK+ MWSEN+	E025-B10	Enable generate WCWRP- on fourth WCFRK+ after WCFSS flip-flop sets
WCWRP-	E025-F10	B44-6 B44-18 B44-31 B46-2 MWSEN+	E025-G7 E031-H10	Trigger WRTPL+ Reset NRZ register to generate longitudinal parity character
WCWRP+	E025-F10	WCWRP-	E025-H10 E025-C5 E026-G8	Reset WCWFM flip-flop on TE Reset WCFSS flip-flop on TE Reset MWSEN flip-flop on TE
Refer to analysis for write one record 2 char/word for exit, starting with detection of RGAPD+				

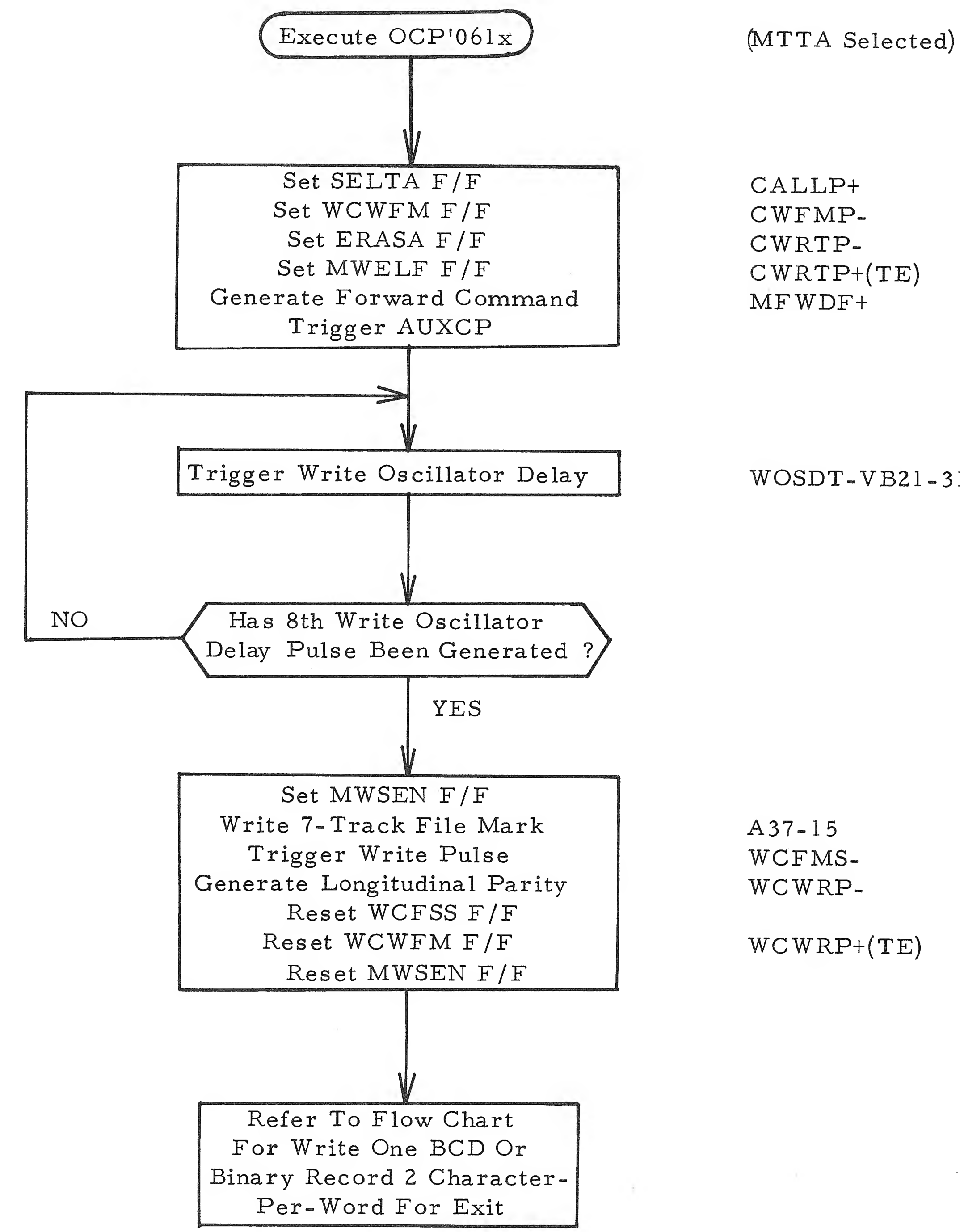


Figure 4-6 Write End Of File - Flow Chart

Forward One Record/Forward One File

(Initiated by OCP'111x or OCP'121x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+A ADB14-A	E010-F10 E010-J5	Enable octal/binary converter Enable generate AOCP1+
AOCP1+	E010-K2	OCPLS+ MTADD+ MBSYS- A1XXX+	E010-K7 E011-A4 E011-A2 E011-A4	Generate CALLP+ Enable generate CFWDP+ Enable generate CSFMP- Enable generate CRERS+
CALLP+	E010-K7	AOCP1+	E013-A3 E014-J3 E015-J3 E016-J3 E017-J3 E023-F10	Reset B45A and B45B flip-flops Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop Reset RCEOF flip-flop
CFWDP+	E011-D4	AX1XX+ AX2XX+ AOCP1+	E013-A5 E013-A7 E013-A5	Reset MREVH flip-flop Set MFWDF flip-flop Enable set MHOLD flip-flop
CRERS+	E011-E6	AX1XX+ AX2XX+ AOCP1+	E018-A4 E019-A4 E020-A4 E021-A4	Enable reset ERASA flip-flop Enable reset ERASB flip-flop Enable reset ERASC flip-flop Enable reset ERASD flip-flop
CSFMP-	E011-A2	AX2XX+ AOCP1+	E023-G10	Set RCSFM flip-flop
MREVH-	E013-A5	CFWDP+	E013-A5	Set MHOLD flip-flop
MFWDF+	E013-A7	CFWDP+	E013-C4 E013-C7 E013-C7	Generate MBSYS+ Generate FWDCM+ Generate SYSRG+
MBSYS+	E013-C4	MFWDF+	E010-F4 E011-F5 E013-C3 E023-G10	Inhibit generate AOCP0- or AOCP1- Motion busy status for SKS'011x Set motion busy extension flip-flop Reset RCSFM flip-flop on TE
RCSFM+	E023-H10	CSFMP-	E023-J9	Enable generate RCEOP-on RCFMD+
RCSFM-	E023-H10	MBSYS+ (TE)	E023-J10	Enable generate RCEOP- on RCEOR+
FWDCM+	E013-C7	MFWDF+ MHOLD- SWPER+ MWELF-	E018-H3 E019-H3 E020-H3 E021-H3	Enable generate TAFWD- Enable generate TBFWD- Enable generate TCFWD- Enable generate TDFWD-

Forward One Record/Forward One File (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
SYSRG+	E013-C8	MFWDF+ MHOLD- SWPER MWELF-	E013-E8 E018-H9 E019-H9 E020-H9 E021-H9	Generate AUXCP+ Enable generate TARDG- Enable generate TBRDG- Enable generate TCRDG- Enable generate TDRDG-
AUXCP+	E013-G8	SYSRG+	E013-H7 E013-D10	Reset RBLKF flip-flop in 2 milli-seconds Reset EOTSF flip-flop
ABUSY+ BBUSY+ CBUSY+ DBUSY+	E013-F3 E013-G3 E013-J3 E013-K3	SELTA+ * SELTB+ B45-5 * SELTC+ * SELTD+ *	E014-E9 E015-E9 E016-E9 E017-E9	Enable generate SBUSY-
WHICK-	E025-A1	STLOD-	E025-C2	Generate WCCLK-
RGECR+	E024-B10	RGCEN+ WCCLK-	E024-C9 E024-J4	Step gap counter Enable generate RCEOR+
RBLKF-	E013-K8	B41-31	E013-J9	Generate RDBLK-
RDBLK-	E013-K9	RBLKF-	E024-B6	Enable set COLLF flip-flop
SBUSY-	E014-F9 E015-F9 E016-F9 E017-F9	ABUSY+ SELTA+A* BBUSY+ SELTB+A* CBUSY+ SELTC+A* DBUSY+ SELTD+A*	E013-E5	Enable set MHOLD flip-flop
STWAT+	E014-F10 E015-F10 E016-F10 E017-F10	TAWAT+ SELTA+A* TBWAT+ SELTB+A* TCWAT+ SELTC+A* TDWAT+ SELTD+A*	E024-A6	Enable set COLLF flip-flop
COLLF+	E024-C6	STWAT+ NTRES- RDBLK-	E024-D6	Trigger collection delay
COLLD+	E024-E6	COLLF+	E024-F6	Set NTRES flip-flop
NTRES+	E024-F6	COLLD+	E024-A1	Trigger read strobe delay
RSDLY-	E024-A1	NTRES+	E024-B1	Generate RSTRB+
RSTRB+	E024-B1	RSDLY-	E022-F8 E023-A10 E023-B9 E023-J1 E023-J2 E024-D1 E024-C4	Clock longitudinal parity checker Enable file mark detector Reset A13C flip-flop on TE Enable generate RCDIP Reset LNHEF flip-flop Set A18E flip-flop Enable set A18B flip-flop if gap detected

*Dependent upon which MTT is selected

Forward One Record/Forward One File (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
RCEOR+	E024-L4	RGCS1+ RGCS2- RGCS3+ RGCS4+ RGCS5+ RGECR+	E023-D10 E023-J10 E024-A4 E024-F2	Enable set RCEOF flip-flop Enable generate RCEOP- Reset RGDET flip-flop Reset RGCEN flip-flop
RCFMD+	E023-C7	A26-7	E023-D10 E023-J9	Enable set RCEOF flip-flop Enable generate RCEOP-
RCEOF-	E023-F10	RCFMD+ RCEOR+	E011-G10	End of file status for SKS'061x
RCEOP-	E023-F10 E023-J9	RCSFM- RCEOR+ or RCFMD+ RCSFM+ RCEOR+	E013-J10	Generate MREST+
RCEOP+	E023-L10	RCEOP-	E013-K8 E023-J4	Reset RBLKF flip-flop on TE Reset READF flip-flop
MREST+	E013-K10	RCEOP+	E013-A7	Reset MFWDF flip-flop
BSYEX+	E013-F1	B45-7	E013-F2 E013-F7	Reset BUSY flip-flops after 8 milli-seconds Reset MHOLD flip-flop
EMINT+	E013-D1	MBSYS+ (TE)	E011-G2	Generate MTINT- if MTMSK flip-flop is set
MTINT-	E011-G2	EMINT+ MTMSK+	E011-K7	Activate PIL00-
CALLP+	E010-K7	AOCP0+ AOCP1+	E013-A3	Deactivate PIL00- on subse- quent magnetic tape OCP

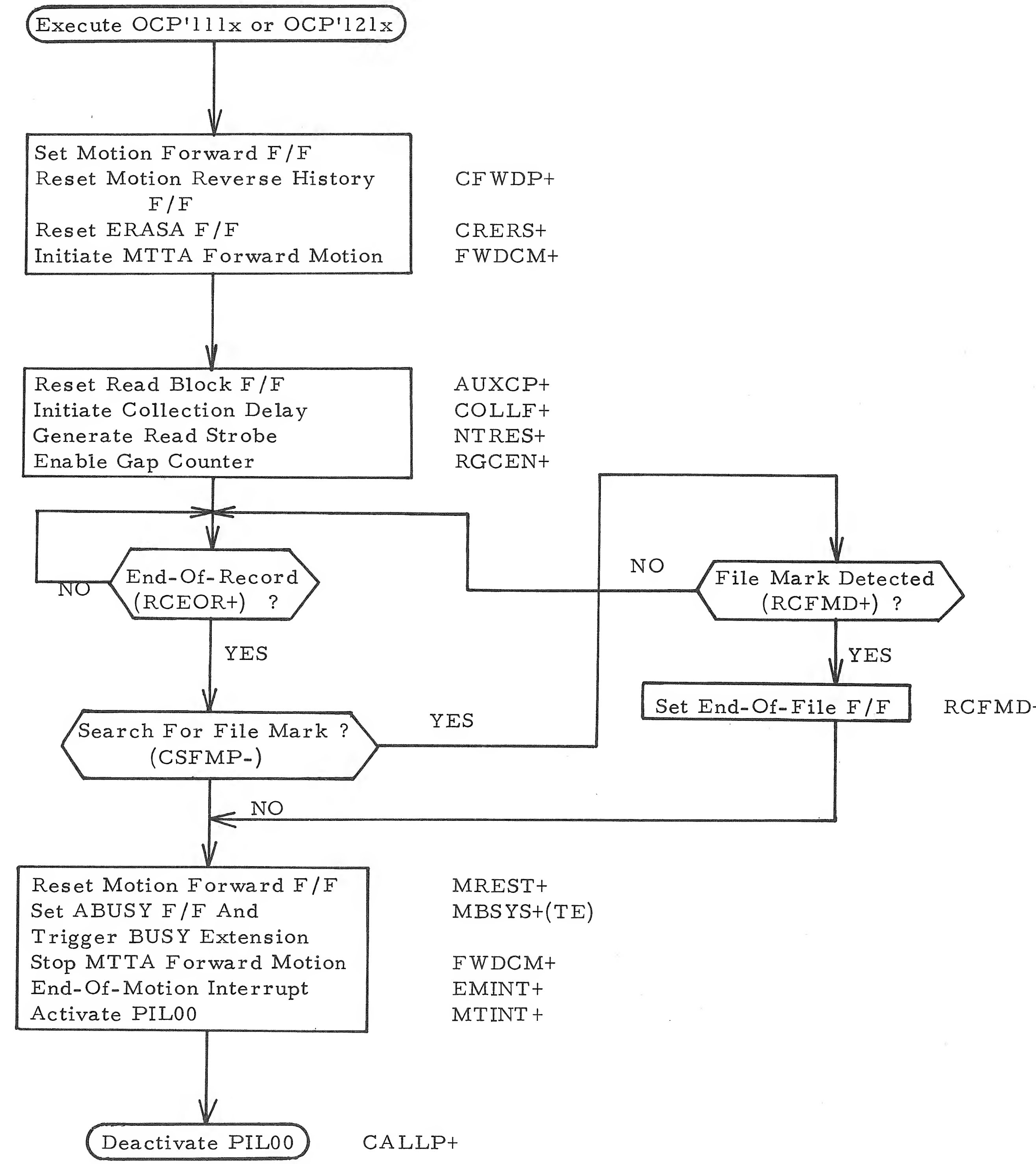


Figure 4-7 Forward One Record/Forward One File - Flow Chart

Back Space One Record/Back Space One File

(Initiated by OCP'151x or OCP'161x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+A ADB14-A	E010-F10 E010-J5	Enable octal/binary converter Enable generate AOCP1+
AOCP1+	E010-K2	OCPLS+ MTADD+ MBSYS- A1XXX+	E010-K7 E011-A7 E011-A2	Generate CALLP+ Enable generate CREVP+ Enable generate CSFMP-
CALLP+	E010-K7	AOCP1+	E013-A3 E014-J3 E015-J3 E016-J3 E017-J3 E023-E10	Reset B45A and B45B flip-flops Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop Reset RCEOF flip-flop
CREVP+	E011-A7	AX5XX- AX6XX- AOCP1+	E013-A5 E013-A9 E013-A6	Set MREVH flip-flop Set MREVF flip-flop if not at load point Enable set MHOLD flip-flop
CREVP-	E011-A7	AX5XX- AX6XX- AOCP1+	E011-E6	Generate CRERS
CSFMP-	E011-A2	AX6XX- AOCP1	E023-G10	Set RCSFM flip-flop
CRERS+	E011-E6	CREVP-	E018-A4 E019-A4 E020-A4 E021-A4	Enable reset ERASA flip-flop Enable reset ERASB flip-flop Enable reset ERASC flip-flop Enable reset ERASD flip-flop
MREVH+	E013-A5	CREVP+	E013-A6	Set MHOLD flip-flop
MREVF+	E013-A10	CREVP+ STLDP-	E013-G9 E013-C9 E013-C9	Enable trigger REVEX- Generate REVCM+ Generate SYSRG+
MREVF-	E013-A10	CREVP+ STLDP-	E013-C4 E023-J1	Generate MBSYS+ Inhibit generate RCDIP+
MBSYS+	E013-C4	MREVF- REVEX-	E010-F4 E011-F5 E013-B3 E023-G10	Inhibit generate AOCP0+ or AOCP1+ Motion busy status for SKS'011x Set motion busy extension flip-flop Reset RCSFM flip-flop on TE
RCSFM+	E023-H10	CSFMP-	E023-J9	Enable generate RCEOP- on RCFMD+ and RCEOR
RCSFM-	E023-H10	MBSYS+ (TE)	E023-J10	Enable generate RCEOP- on RCEOR+

Back Space One Record/Back Space One File (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
REVCM+	E013-C9	MREVF+ MHOLD-	E018-H4 E019-H4 E020-H4 E021-H4	Enable generate TAREV- Enable generate TBREV- Enable generate TCREV- Enable generate TDREV-
SYSRG+	E013-C8	MREVF+ MHOLD-	E013-E8 E018-H9 E019-H9 E020-H9 E021-H9	Generate AUXCP+ Enable generate TARDG- Enable generate TBRDG- Enable generate TCRDG- Enable generate TDRDG-
AUXCP+	E013-G8	SYSRG+	E013-H7	Reset RBLKF flip-flop in 2 milli-seconds
ABUSY+ BBUSY+ CBUSY+ DBUSY+	E013-F3 E013-G3 E013-J3 E013-K3	SELTA+ * SELTB+ B45-5 * SELTC+ * SELTD+ *	E014-E9 E015-E9 E016-E9 E017-E9	Enable generate SBUSY-
WHICK-	E025-A1	STLOD-	E025-C2	Generate WCCLK-
RGECR+	E024-B10	RGCEN+ WCCLK-	E024-C9 E024-J4	Step gap counter Enable generate RCEOR
RBLKF-	E013-K8	B41-31	E013-J9	Generate RDBLK-
RDBLK-	E013-K9	RBLKF-	E024-B6	Enable set COLLF flip-flop
SBUSY-	E014-F9 E015-F9 E016-F9 E017-F9	ABUSY+ SELTA+A* BBUSY+ SELTB+A* CBUSY+ SELTC+A* DBUSY+ SELTD+A*	E013-D5	Enable set MHOLD flip-flop
STWAT+	E014-F10 E015-F10 E016-F10 E017-F10	TAWAT+ SELTA+A* TBWAT+ SELTB+A* TCWAT+ SELTC+A* TDWAT+ SELTD+A*	E024-	Enable set COLLF flip-flop
COLLF+	E024-C6	STWAT+ NTRES- RDBLK-	E024-D6	Trigger collection delay
COLLD+	E024-E6	COLLF+	E024-F6	Set NTRES flip-flop
NTRES+	E024-F6	COLLD+	E024-A1	Trigger read strobe delay
RSDLY-	E024-A1	NTRES+	E024-B1	Generate RSTRB+
RSTRB+	E024-B1	RSDLY-	E022-F8 E023-A10 E023-B9 E023-K2 E024-D1	Clock longitudinal parity checker Enable file mark detector Reset A13C flip-flop on TE Reset LNHEF flip-flop Set A18E flip-flop

* Dependent upon which MTT is selected

Back Space One Record/Back Space One File (Continued)

Signal	Origin	Signal Component	Destination	Operation Description
RSTRB+	E024-B1	RSDLY-	E024-C4	Enable set A18B flip-flop if gap detected
RCEOR+	E024-L4	RGCS1+ RGCS2- RGCS3+ RGCS4+ RGCS5+ RGECR+	E023-D10 E023-J10 E024-A4 E024-F2	Enable set RCEOF flip-flop Enable generate RCEOP- Reset RGDET flip-flop Reset RGCEN flip-flop
RCFMD+	E023-C7	A26-7	E023-D10	Enable set RCEOF flip-flop
RCEOF-	E023-F10	RCFMD+ RCEOR+	E011-G10	End of file status for SKS'061x
RCEOP-	E023-J10 E023-J9	RCSFM- RCEOR+ or RCFMD+ RCSFM- RCEOR+	E013-K10 E027-F8 E013-J8	Generate MREST- Reset BXFCF flip-flop Reset RBLKF flip-flop on TE
RCEOP+	E023-L10	RCEOP-	E013-F9 E023-J4	Trigger REVEX- Reset READF flip-flop
MREST+	E013-K10	RCEOP+	E013-A10	Reset MREVF flip-flop
MREVF-	E013-A10	MREST+ STLDP-	E013-B10 E013-C4	Disable reverse command Remove MBSYS+ to trigger BSYEX+ and generate EMINT+
BSYEX+	E013-F1	B45-7	E013-F2 E013-F7	Reset BUSY flip-flop after 8 milli-seconds Reset MHOLD flip-flop
EMINT+	E013-D1	MBSYS (TE)	E011-G2	Generate MTINT- if MTMSK flip-flop is set
MTINT-	E011-G2	EMINT+ MTMSK+	E011-K7	Activate PIL00-
CALLP+	E010-K7	AOCP0+ AOCP1+	E013-A3	Deactivate PIL00- on subsequent magnetic tape OCP

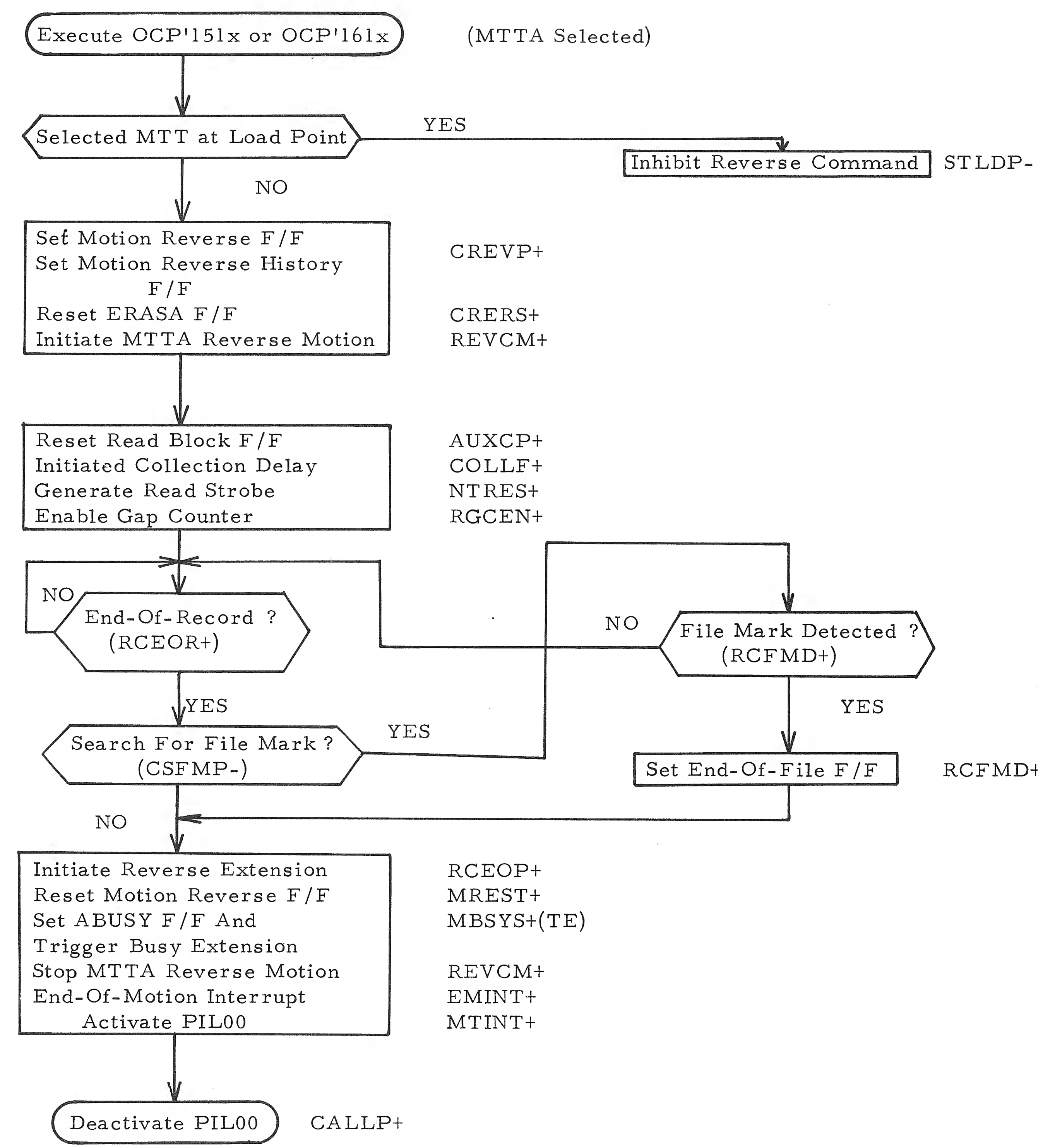


Figure 4-8 Back Space One Record/Back Space One File - Flow Chart

Tape Rewind

(Initiated by OCP'141x)

Signal	Origin	Signal Component	Destination	Operation Description
OCPLS+	E010-J3	OCPLS-	E010-K3	Output control pulse from CP
MTADD+	E010-B3	ADB11- ADB12- ADB13+ ADB14-A	E010-F10 E010-J5	Enable octal/binary converter Enable generate AOCP1+
AOCP1+	E010-K2	OCPLS+ MTADD+ MBSYS- A1XXX+	E010-K7 E011-D9	Generate CALLP+ Enable generate CRWDP+
CALLP+	E010-K7	AOCP1+	E013-A3 E014-J3 E015-J3 E016-J3 E017-J3	Reset B45A and B45B flip-flops Set/Reset SELTA flip-flop Set/Reset SELTB flip-flop Set/Reset SELTC flip-flop Set/Reset SELTD flip-flop
CRWDP-	E011-B7	AOCP1+ AX4XX+	E011-E6	Generate CRERS+
CRWDP+	E011-B7	CRWDP-	E013-G5	Set RWDCM flip-flop
CRERS+	E011-E6	CRWDP-	E018-A4 E019-A4 E020-A4 E021-A4	Enable reset ERASA flip-flop Enable reset ERASB flip-flop Enable reset ERASC flip-flop Enable reset ERASD flip-flop
RWDCM+	E013-G5	CRWDP+	E013-J5 E018-A9 E019-A9 E020-A9 E021-A9	Initiate 120 milli-second delay if not at load point Enable generate TARWD+ and set SARWD flip-flop Enable generate TBRWD+ and set SBRWD flip-flop Enable generate TCRWD+ and set SCRWD flip-flop Enable generate TDRWD+ and set SDRWD flip-flop
RWDCM	E013-G5	CRWDP+	E013-C4 E013-E8	Generate MBSYS+ Generate AUXCP+
MBSYS+	E013-C4	RWDCM-	E010-F4 E011-F5 E013-B3	Inhibit generate AOCP0+ or AOCP1+ Motion busy status for SKS-011x Set motion busy extension flip-flop
TARWD+ TBRWD+ TCRWD+ TDRWD+	E018-D7 E019-D7 E020-D7 E021-D7	RWDCM+ SELTA+* RWDCM+ SELTB+* RWDCM+ SELTC+* RWDCM+ SELTD+*	MTTA MTTB MTTC MTTD	MTTA rewind command MTTB rewind command MTTC rewind command MTTD rewind command

* Dependent upon which MTT is selected

Tape Rewind (Continued)

Signal	Origin	Signal Command	Destination	Operation Description
SARWD+ SBRWD+ SCRWD+ SDRWD+	E018-D9 E019-D9 E020-D9 E021-D9	RWDCM+ SELTA+* RWDCM+ SELTB+* RWDCM+ SELTC+* RWDCM+ SELTD+*	E018-E8 E019-E8 E020-E8 E021-E8	Enable generate SRWDS- Enable generate SRWDS- Enable generate SRWDS- Enable generate SRWDS-
SARWD- SBRWD- SCRWD- SDRWD-	E018-D9 E019-D9 E020-D9 E021-D9	RWDCM+ SELTA+* RWDCM+ SELTB+* RWDCM+ SELTC+* RWDCM+ SELTD+*	E013-A1	Generate EMINT on TE
AUXCP+	E013-G8	RWDCM-	E013-J5 E013-J7	Initiate 120 milli-seconds delay Reset RDBLK in 2 milli-seconds
ABUSY+ BBUSY+ CBUSY+ DBUSY+	E013-F3 E013-G3 E013-J3 E013-K3	SELTA+ * SELTB+ B45-5 * SELTC+ * SELTD+ *	E014-E9 E015-E9 E016-E9 E017-E9	Enable generate SBUSY-
SRWDS-	E018-E8 E019-E8 E020-E8 E021-E8	AADDC+ C24-7 * BADDC+ C24-19 * CADDC+ C53-7 * DADDC+ C57-19 *	E011-H1	Select rewind status for SKS'141x
STLDP-	E014-D10 E015-D10 E016-D10 E017-D10	TABOT+ SELTA+ * TBBOT+ SELTB+ * TCBOT+ SELTC+ * TDBOT+ SELTD+ *	E013-G6 E011-G8	Reset RWDCM flip-flop Selected load point for SKS'031x
EMINT+	E018-D1	B45-1 B45-5	E011-G2	Generate MTINT- if MTMSK flip-flop is set
MTINT-	E011-G2	EMINT+ MTMSK+	E011-K7	Activate PIL00-
CALLP+	E010-K7	AOCP0+ AOCP1-	E013-A3	Deactivate PIL00- on subsequent magnetic tape OCP

* Dependent upon which MTT is selected

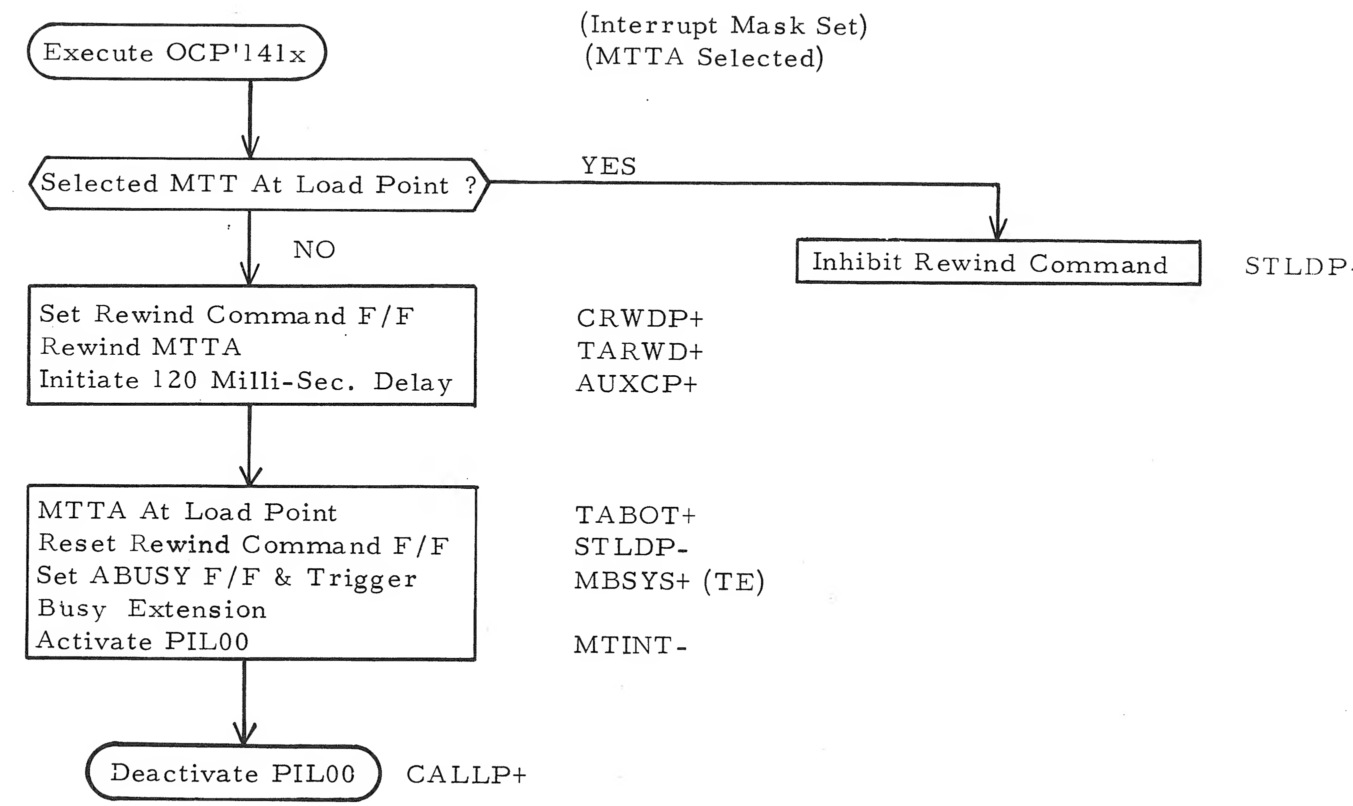
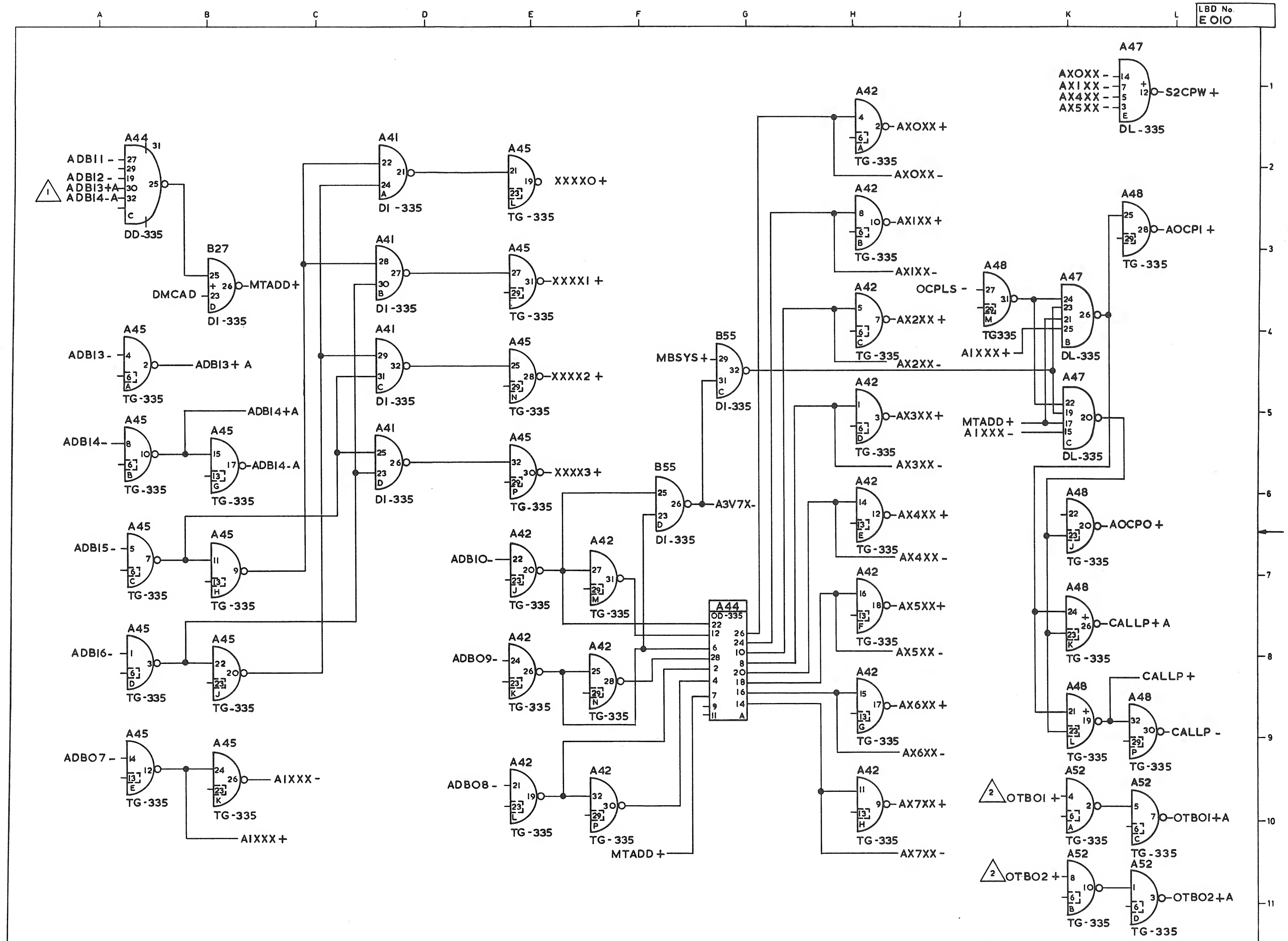


Figure 4-9 Tape Rewind - Flow Chart



1. FOR A SECOND TCU EXCHANGE ADB14 - A WITH ADB14 + A

2. IF DMA CONNECTIONS ARE MADE OTB01+ AND OTB02+ ARE PICKED UP AT I/O BUS OF NEAREST OPTION.

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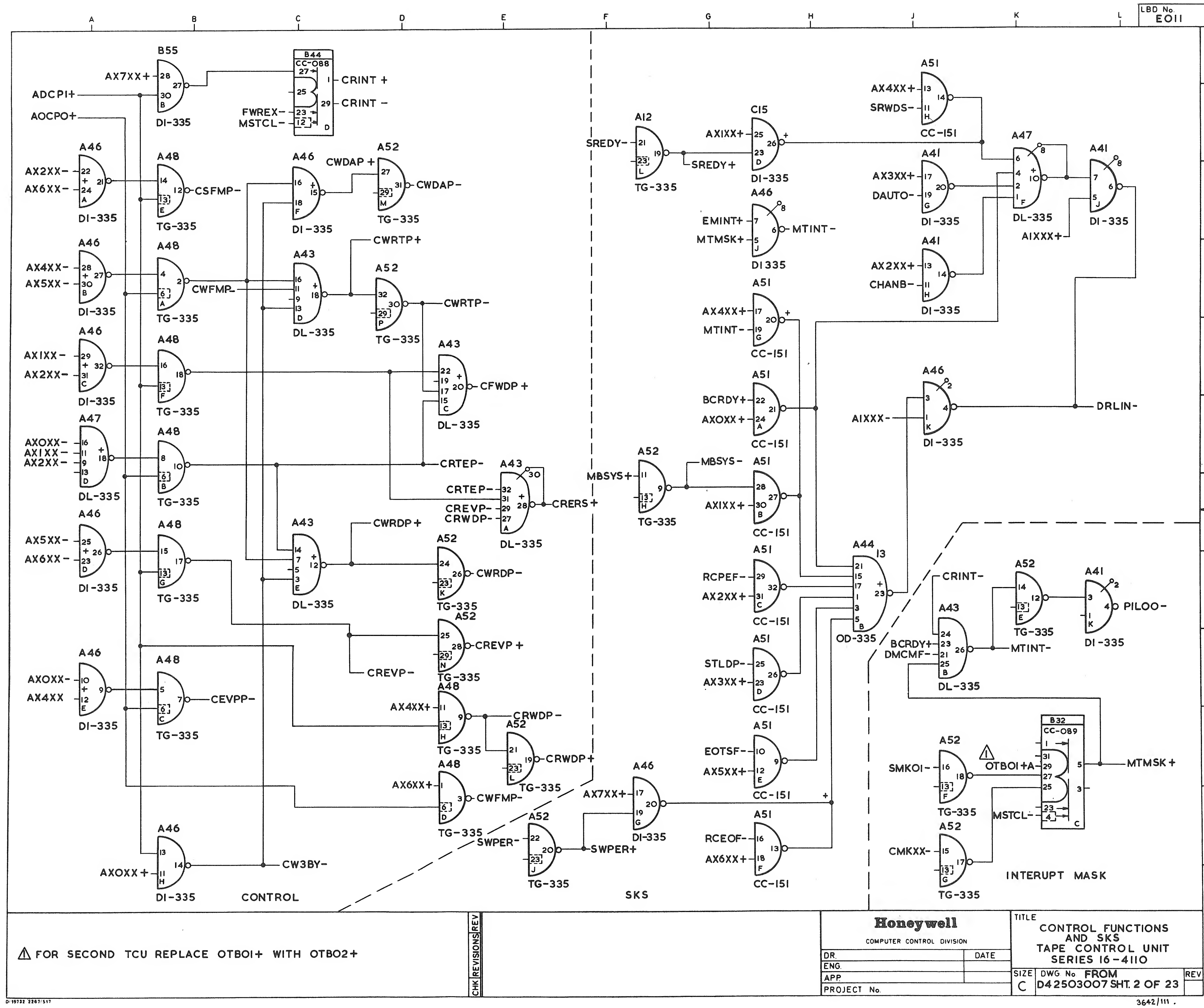
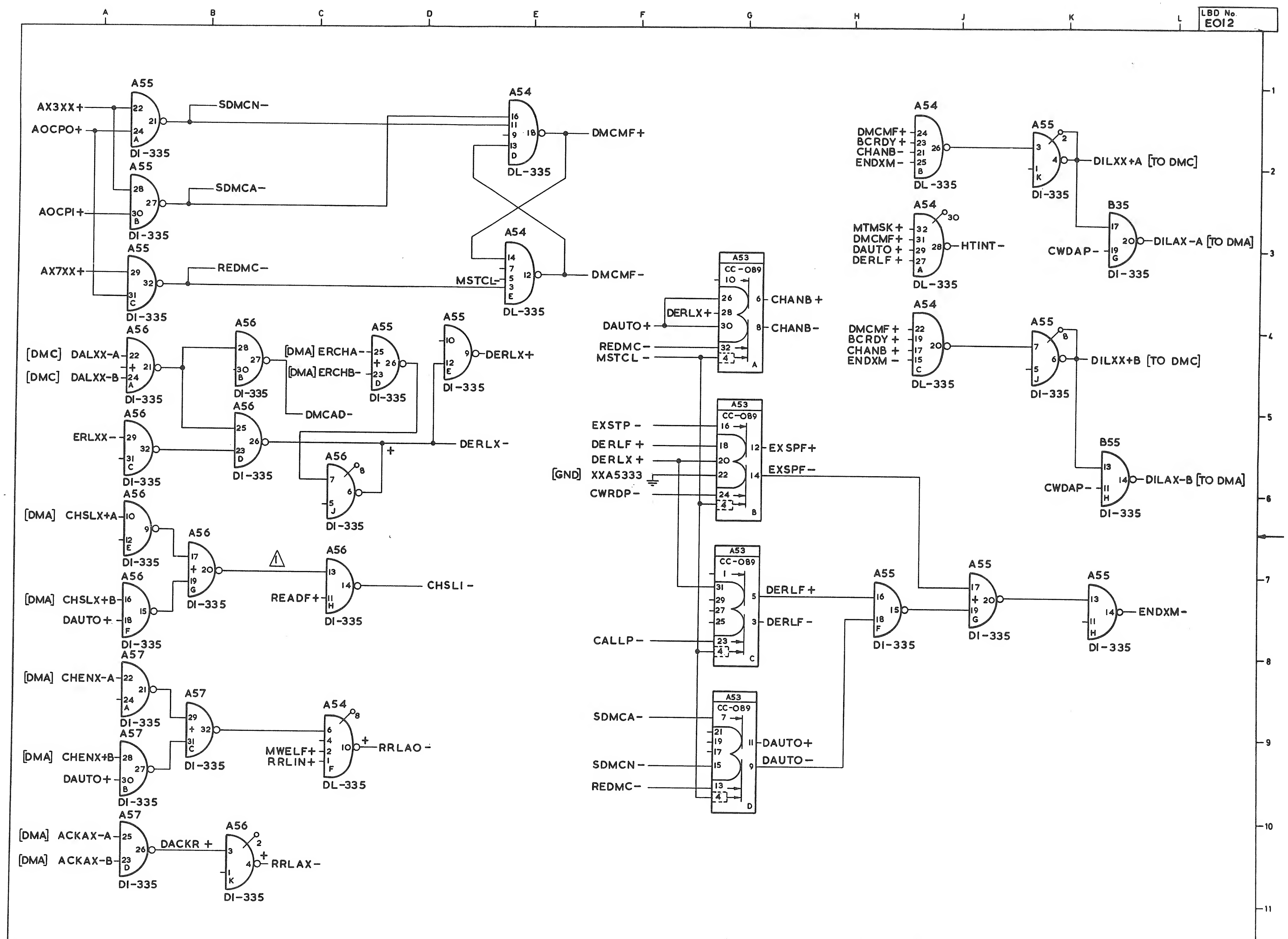
Honeywell
COMPUTER CONTROL DIVISION

DR.	DATE
ENG	
APP	
PROJECT No.	

TITLE
ADDRESS BUS DECODER
TAPE CONTROL UNIT
SERIES 16 - 4110

SIZE	DWG No.	FROM	REV
C	D42503007 SHT. 1 OF 23		


LBD No. E011
CONTROL
SKS
INTERUPT MASK
⚠ FOR SECOND TCU REPLACE OTB01+ WITH OTB02+
Honeywell
COMPUTER CONTROL DIVISION
CONTROL FUNCTIONS AND SKS
TAPE CONTROL UNIT
SERIES 16-4110
SIZE C
DWG No. FROM D42503007 SHT. 2 OF 23



FOR DMC OPTION [4160] CONNECT A5613 TO A5633 [GND]

LBD No
E012

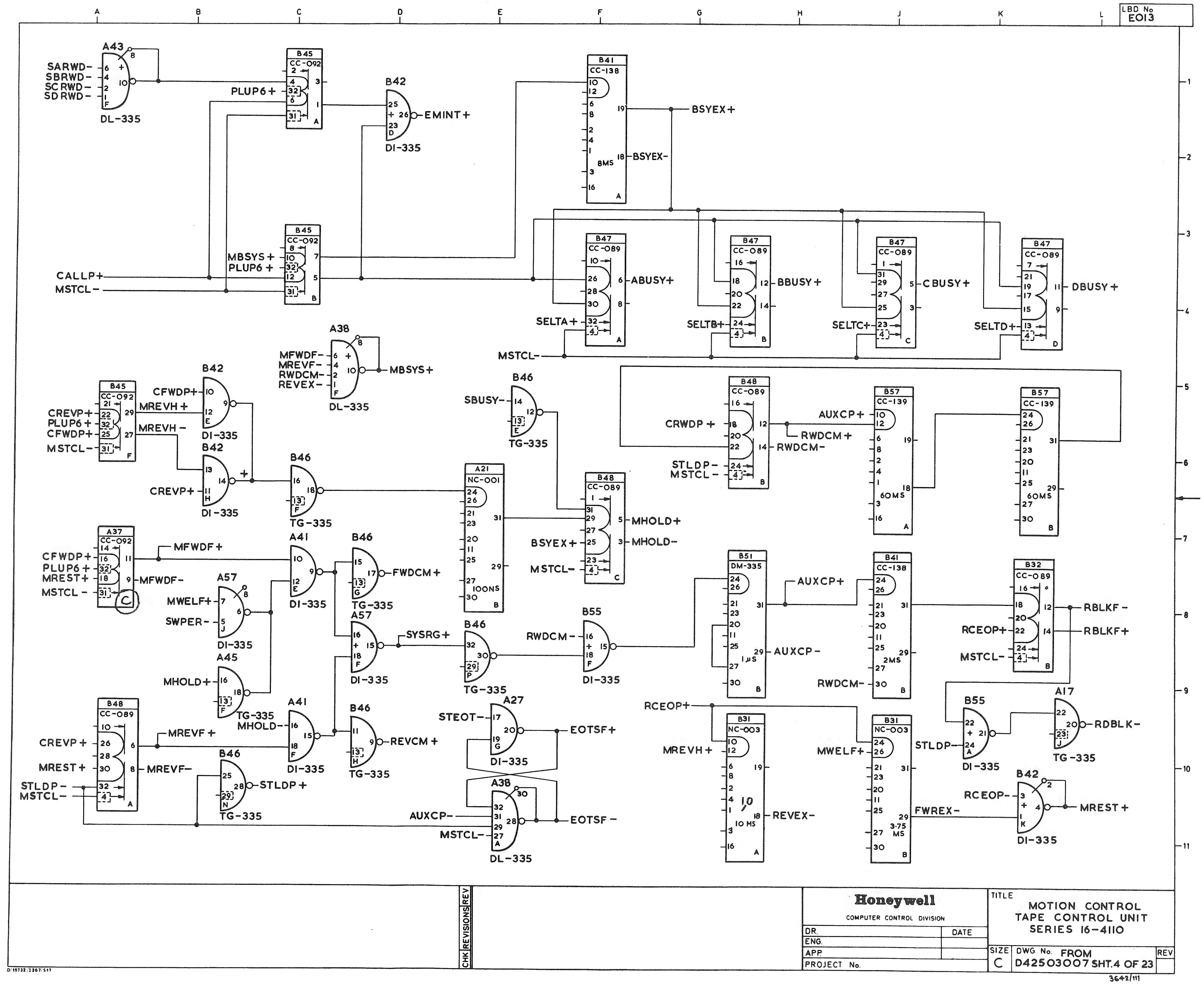
Honeywell
COMPUTER CONTROL DIVISION

TITLE
DMC/DMA SUB-CHANNEL
TAPE CONTROL UNIT
SERIES 16-4110

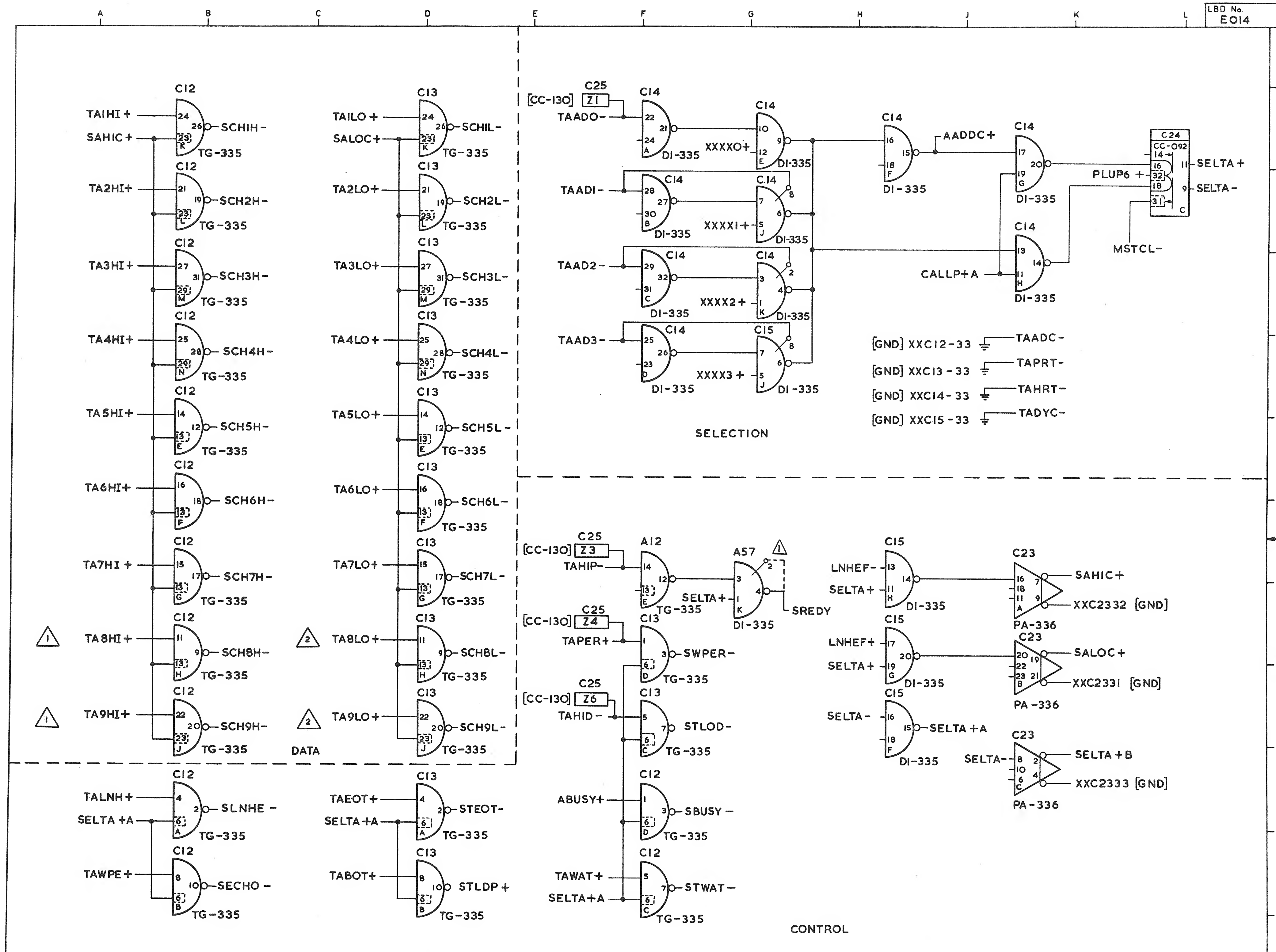
SIZE C — DWG No FROM D42503007 SHT. 3 OF 23

DR / ENG / APP / PROJECT No. / DATE / CHK / REVISIONS / REV

3642/111



LBD No E013
SARWD-
SBRWD-
SCRWD-
SDRWD-
A43
DL-335
B45
CC-092
PLUP6+
B42
DI-335
EMINT+
B41
CC-138
8MS
BSYEX+
BSYEX-
CALLP+
MSTCL-
MBSYS+
PLUP6 +
B47
CC-089
ABUSY+
BBUSY+
CBUSY+
DBUSY+
SELTA+
SELTB+
SELTC+
SELTD+
A38
MFWDF-
MREVF-
RWDCM-
REVEX-
MBSYS+
CREVP+
PLUP6+
CFWDP+
CFWDP+
MREVH+
MREVH-
B46
TG-335
SBUSY-
A21
NC-001
100NS
B48
MHOLD+
MHOLD-
BSYEX+
CRWDP+
AUXCP+
RWDCM+
RWDCM-
STLDP-
B57
CC-139
60MS
A37
MFWDF+
MFWDF-
MREST+
A57
MWELF+
SWPER-
A41
FWDCM+
SYSRG+
A45
MHOLD+
MHOLD-
B51
DM-335
1μS
AUXCP-
B55
RWDCM-
2MS
B32
RBLKF-
RBLKF+
RCEOP+
STEOT-
A27
EOTSF+
EOTSF-
REVCM+
MREVF+
MREVF-
STLDP+
AUXCP-
RCEOP+
B31
NC-003
MREVH+
10 MS
REVEX-
MWELF+
3.75 MS
FWREX-
A17
RDBLK-
RCEOP-
MREST+
Honeywell
COMPUTER CONTROL DIVISION
TITLE
MOTION CONTROL
TAPE CONTROL UNIT
SERIES 16-4110
DR.
ENG.
APP
PROJECT No.
DATE
SIZE C
DWG No. FROM D42503007 SHT.4 OF 23
REV
CHK REVISIONS REV



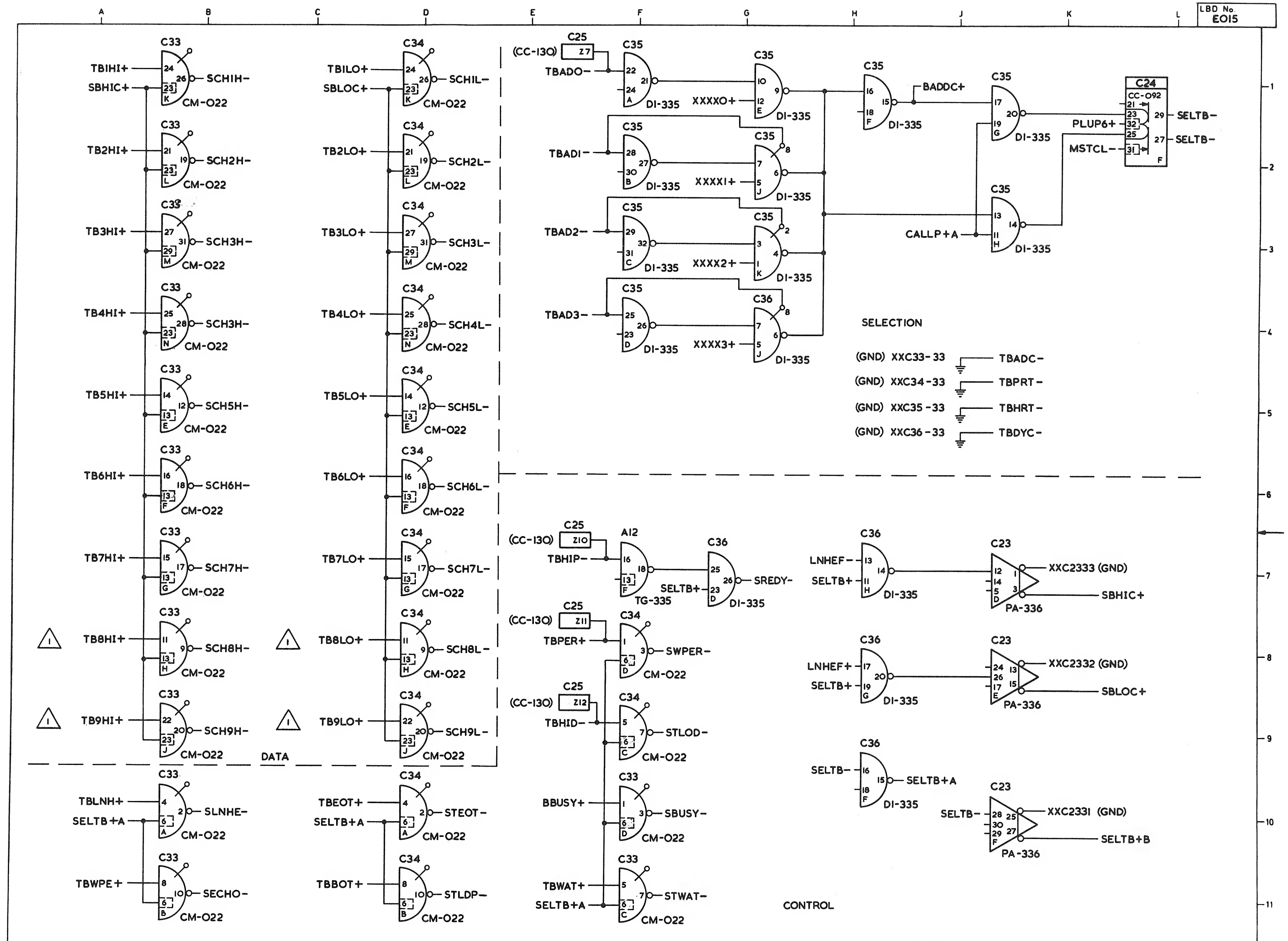
1 DELETE A5702 TO A5704 FOR DUAL, TRIPLE OR QUADRUPLE INSTALLATION

2 NOT USED

Honeywell COMPUTER CONTROL DIVISION	TITLE FIRST UNIT SELECTION TAPE CONTROL UNIT SERIES 16-4110
DR / ENG / APP / PROJECT No. / DATE	SIZE C DWG No. FROM D42503007 SHT. 5 OF 23 REV

3642/111

LBD No. E015



NOT USED

REVISIONS | REV | CHK

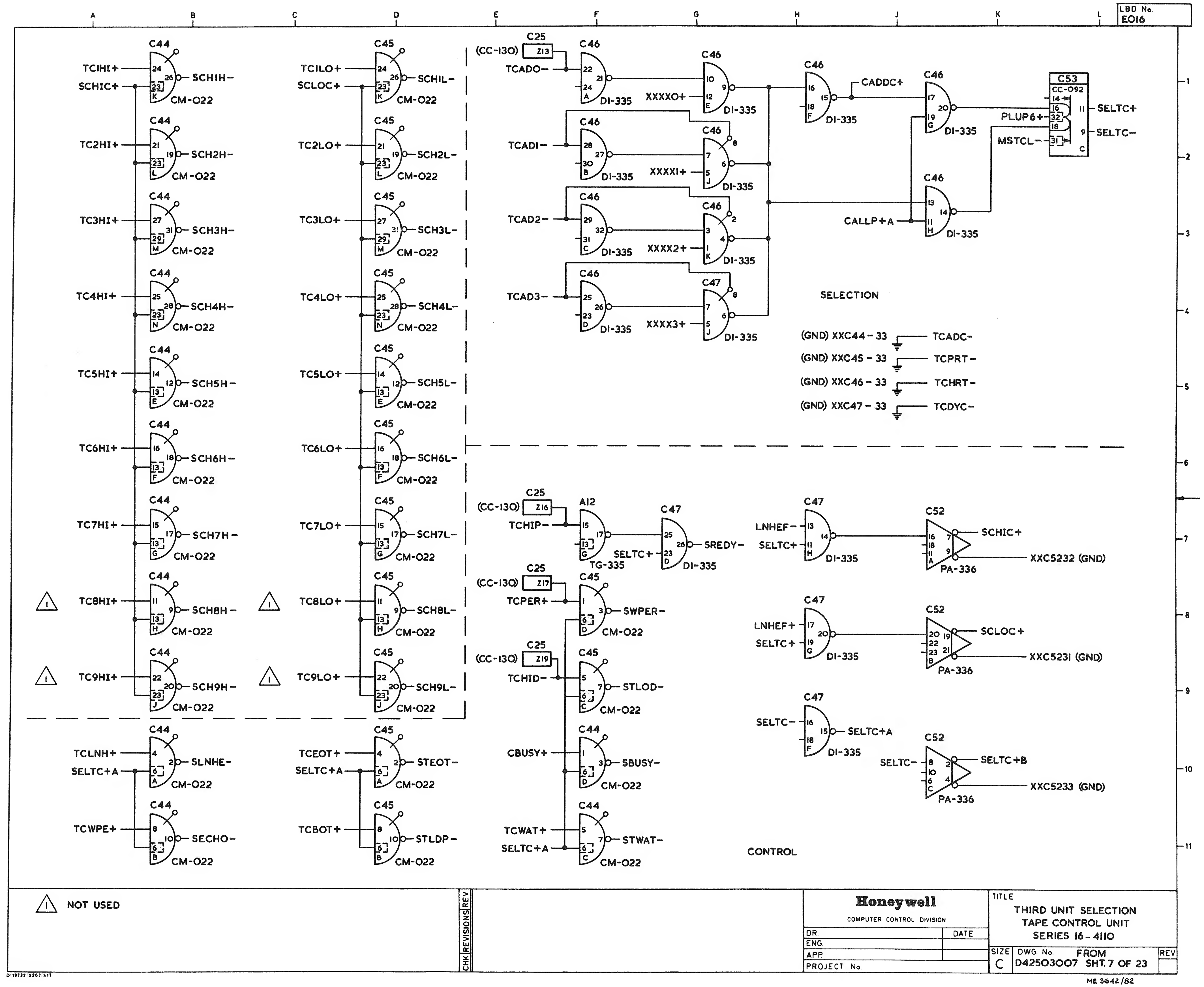
Honeywell
COMPUTER CONTROL DIVISION

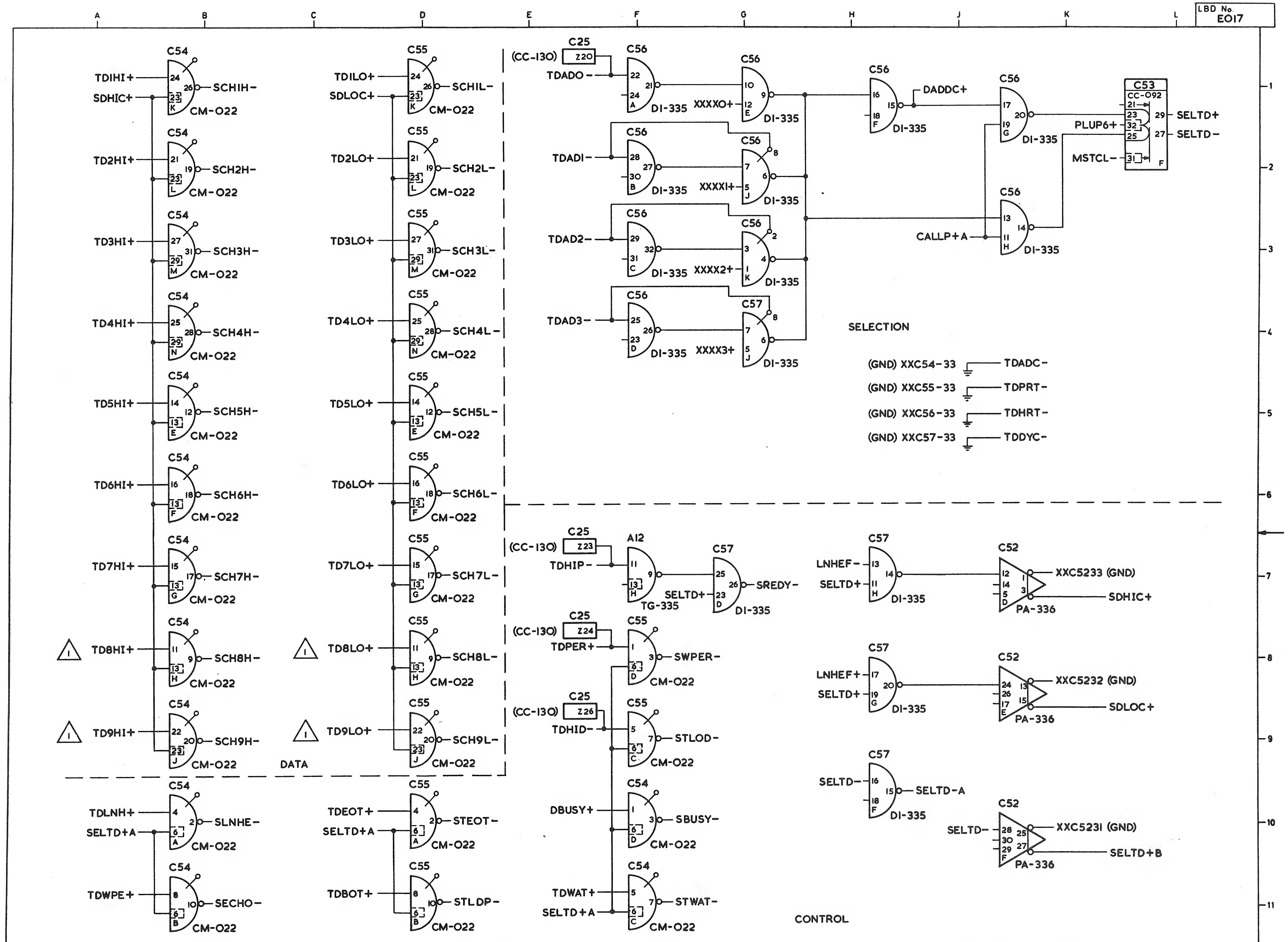
DR.	DATE
ENG.	
APP	
PROJECT No.	

TITLE SECOND UNIT SELECTION
TAPE CONTROL UNIT
SERIES 16-4110

SIZE	DWG No.	FROM	REV
C	D42503007	SHT. 6 OF 23	

ME 3642/82


LBD No. E016
TC1HI+
SCHIC+
SCH1H-
CM-022
TC2HI+
SCH2H-
TC3HI+
SCH3H-
TC4HI+
SCH4H-
TC5HI+
SCH5H-
TC6HI+
SCH6H-
TC7HI+
SCH7H-
TC8HI+
SCH8H-
TC9HI+
SCH9H-
TC1LO+
SCLOC+
SCH1L-
TC2LO+
SCH2L-
TC3LO+
SCH3L-
TC4LO+
SCH4L-
TC5LO+
SCH5L-
TC6LO+
SCH6L-
TC7LO+
SCH7L-
TC8LO+
SCH8L-
TC9LO+
SCH9L-
TCLNH+
SELTC+A
SLNHE-
TCWPE+
SECHO-
TCEOT+
STEOT-
TCBOT+
STLDP-
(CC-130)
TCADO-
TCAD1-
TCAD2-
TCAD3-
XXXX0+
XXXX1+
XXXX2+
XXXX3+
DI-335
CADDC+
CALLP+A
PLUP6+
MSTCL-
CC-092
SELTC+
SELTC-
SELECTION
(GND) XXC44 - 33
TCADC-
(GND) XXC45 - 33
TCPRT-
(GND) XXC46 - 33
TCHRT-
(GND) XXC47 - 33
TCDYC-
TCHIP-
TG-335
SREDY-
TCPER+
SWPER-
TCHID-
STLOD-
CBUSY+
SBUSY-
TCWAT+
STWAT-
LNHEF-
SCHIC+
XXC5232 (GND)
PA-336
LNHEF+
SCLOC+
XXC5231 (GND)
SELTC+B
XXC5233 (GND)
CONTROL
NOT USED
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR
DATE
ENG
APP
PROJECT No.
TITLE
THIRD UNIT SELECTION
TAPE CONTROL UNIT
SERIES 16-4110
SIZE C
DWG No D42503007
FROM SHT. 7 OF 23
REV
ME 3642/82



△ NOT USED

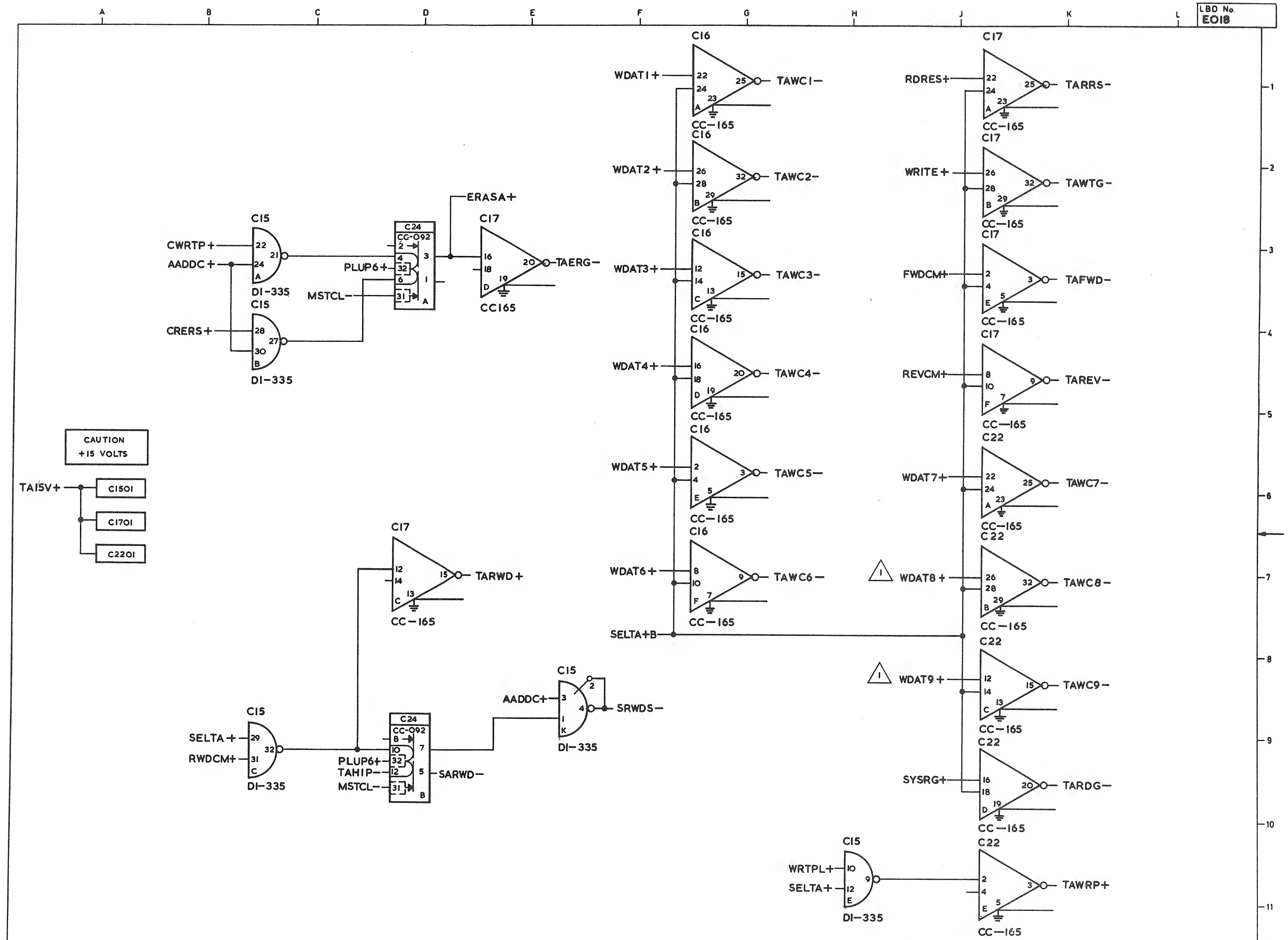
Honeywell
COMPUTER CONTROL DIVISION

DR.	DATE
ENG.	
APP.	
PROJECT No.	

TITLE
FOURTH UNIT SELECTION
TAPE CONTROL UNIT
SERIES 16 - 4110

SIZE	DWG. No.	FROM	REV
C	D42503007	SHT. 8 OF 23	

ME 3642/82



Honeywell

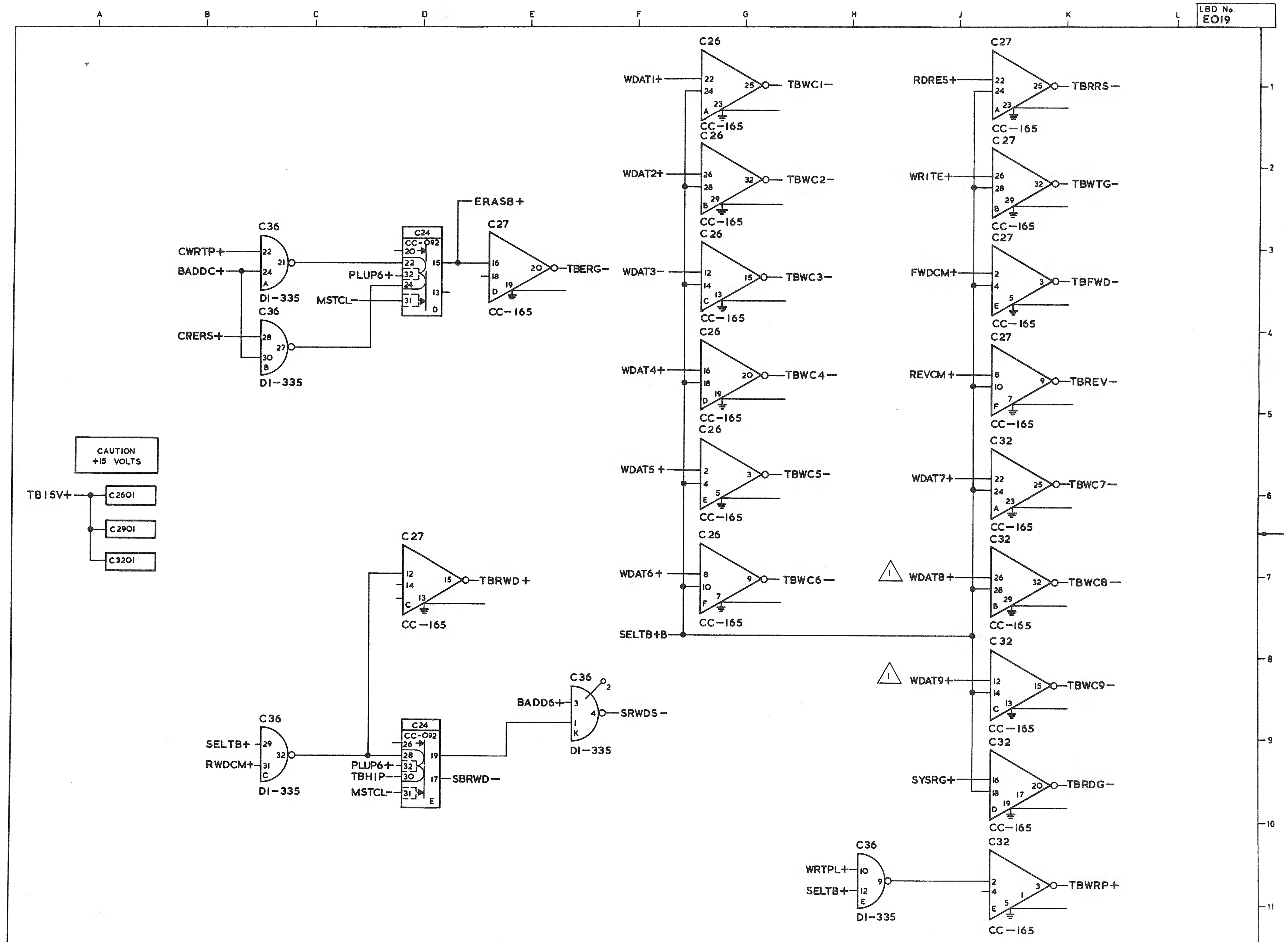
COMPUTER CONTROL DIVISION

DR.	DATE
ENG.	
APP	
PROJECT No.	

TITLE
FIRST UNIT DRIVERS.
TAPE CONTROL UNIT
SERIES 16−4110.

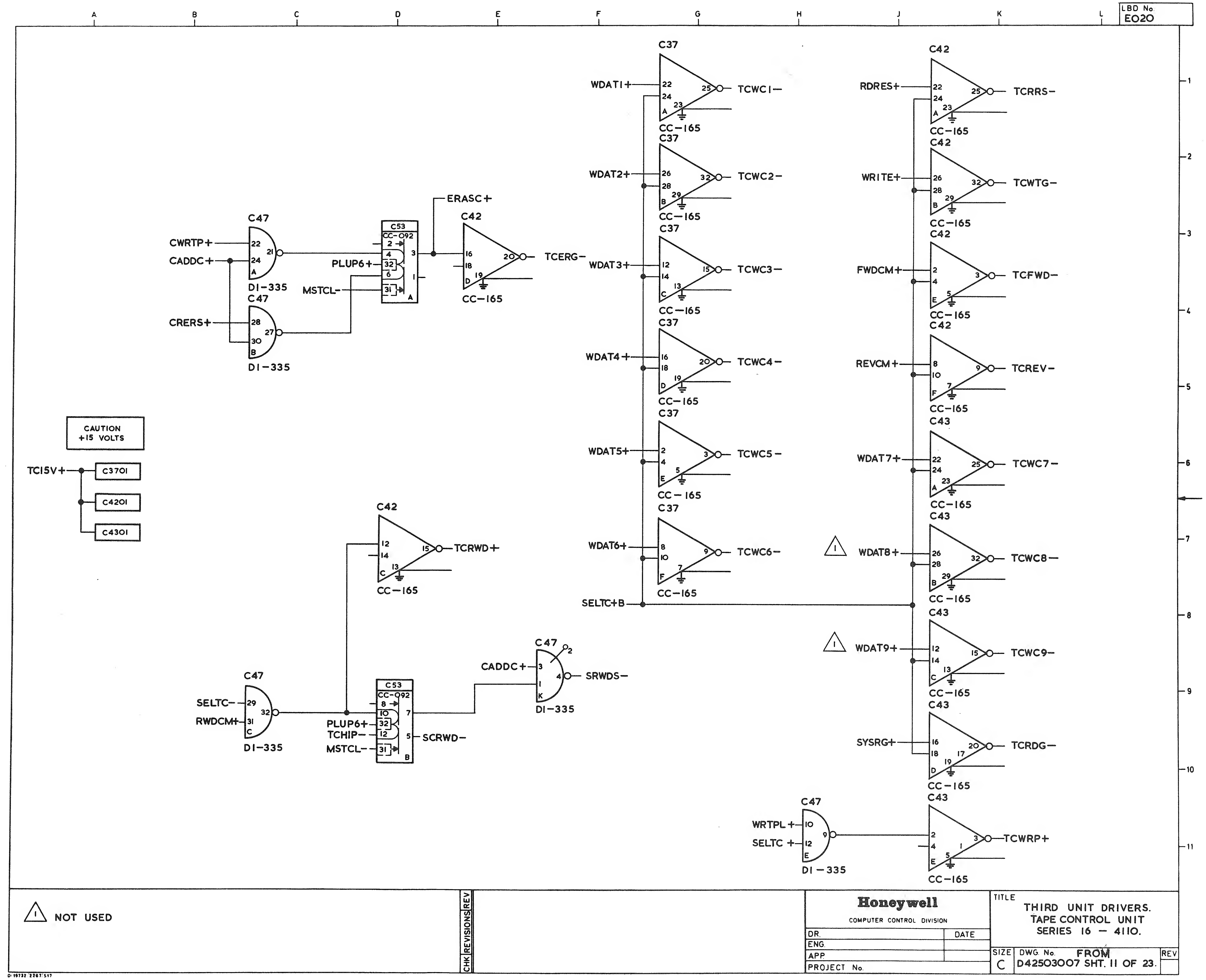
SIZE	DWG No.	FROM	REV
C	D42503007 SHT. 9 OF 23.		

CHK REVISIONS REV

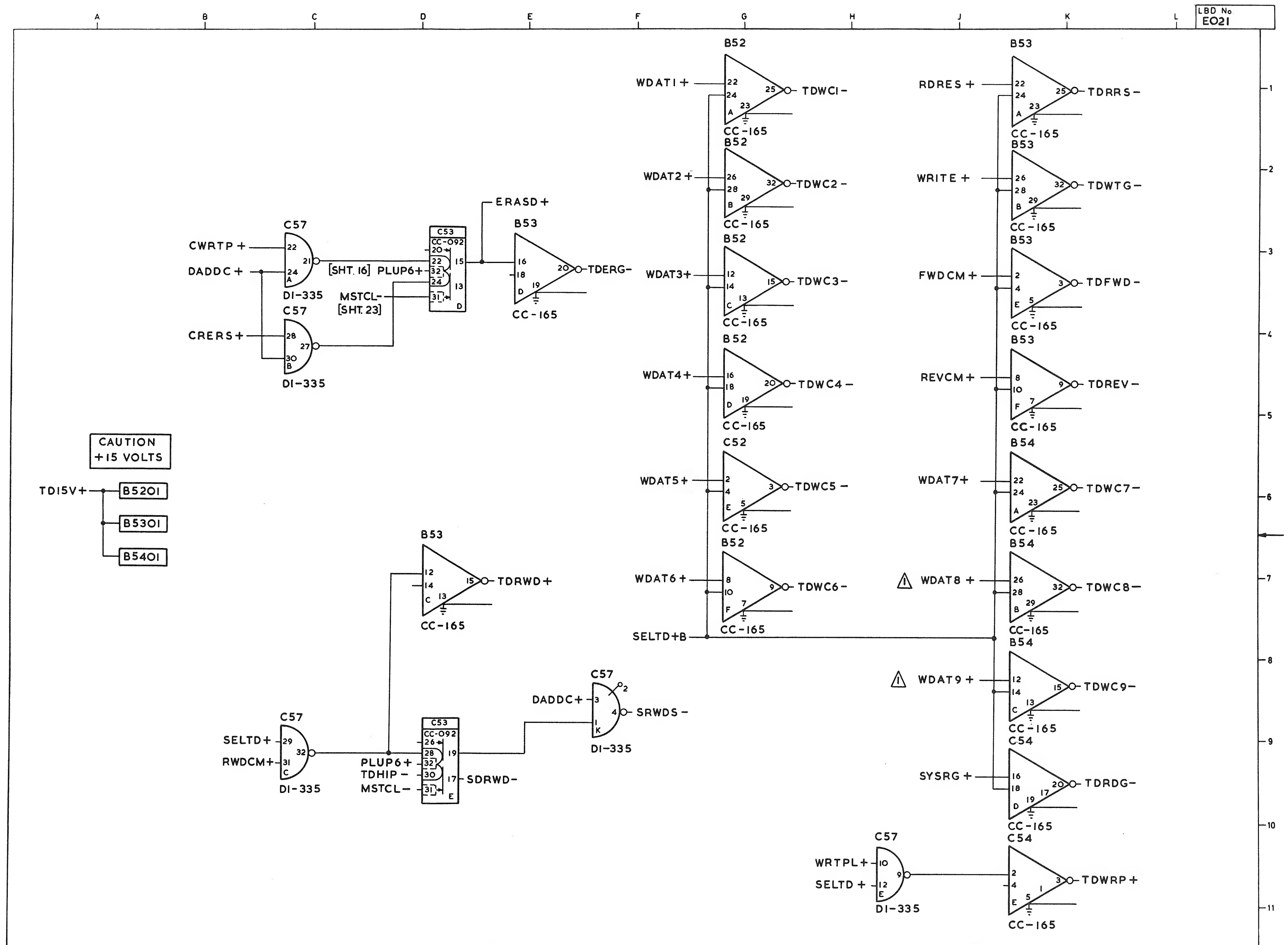


NOT USED

Honeywell COMPUTER CONTROL DIVISION	TITLE SECOND UNIT DRIVERS TAPE CONTROL UNIT SERIES 16 − 4110
DR / ENG / APP / PROJECT No. / DATE	SIZE C — DWG No. D42503007 — FROM SHT. 10 OF 23. — REV



LBD No
E020
CAUTION
+15 VOLTS
TC15V+
C3701
C4201
C4301
CWRTP+
CADDC+
CRERS+
C47
D1-335
C53
CC-092
PLUP6+
MSTCL-
ERASC+
C42
CC-165
TCERG-
TCRWD+
SELTC-
RWDCM+
TCHIP-
SCRWD-
SRWDS-
WDAT1+
TCWC1-
WDAT2+
TCWC2-
WDAT3+
TCWC3-
WDAT4+
TCWC4-
WDAT5+
TCWC5-
WDAT6+
TCWC6-
SELTC+B
C37
RDRES+
TCRRS-
WRITE+
TCWTG-
FWDCM+
TCFWD-
REVCM+
TCREV-
WDAT7+
TCWC7-
WDAT8+
TCWC8-
WDAT9+
TCWC9-
SYSRG+
TCRDG-
C43
WRTPL+
SELTC+
TCWRP+
NOT USED
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR.
DATE
ENG.
APP
PROJECT No.
TITLE
THIRD UNIT DRIVERS.
TAPE CONTROL UNIT
SERIES 16 — 4110.
SIZE C
DWG. No. FROM
D42503007 SHT. 11 OF 23.
REV



NOT USED

CHK REVISIONS REV

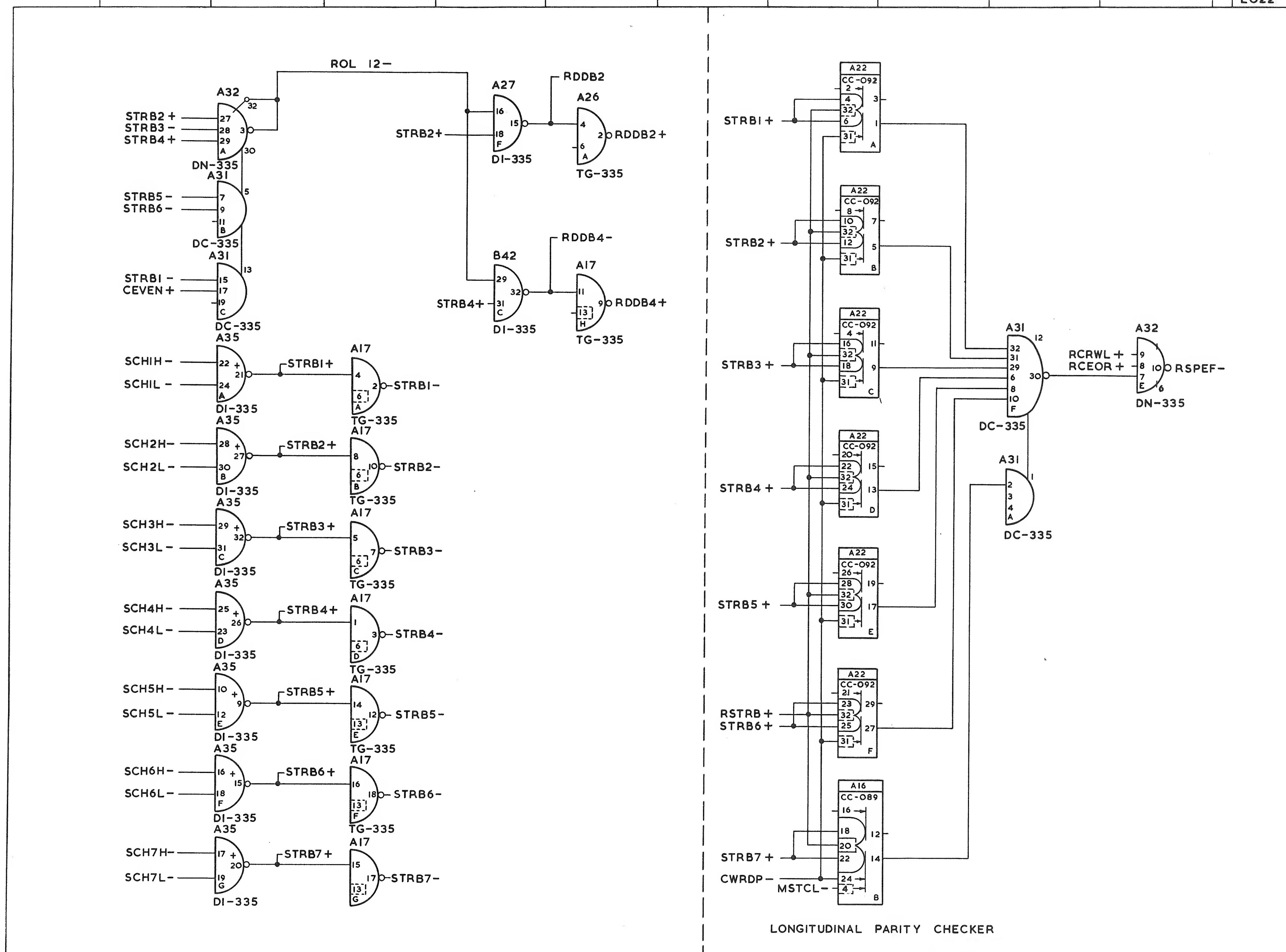
Honeywell
COMPUTER CONTROL DIVISION

DR.	DATE
ENG.	
APP	
PROJECT No.	

TITLE
FOURTH UNIT DRIVERS
TAPE CONTROL UNIT
SERIES 16-4110

SIZE C DWG No. FROM D42503007 SHT. 12 OF 23 REV

LBD No. E022



REVISIONS | REV | CHK

Honeywell
COMPUTER CONTROL DIVISION

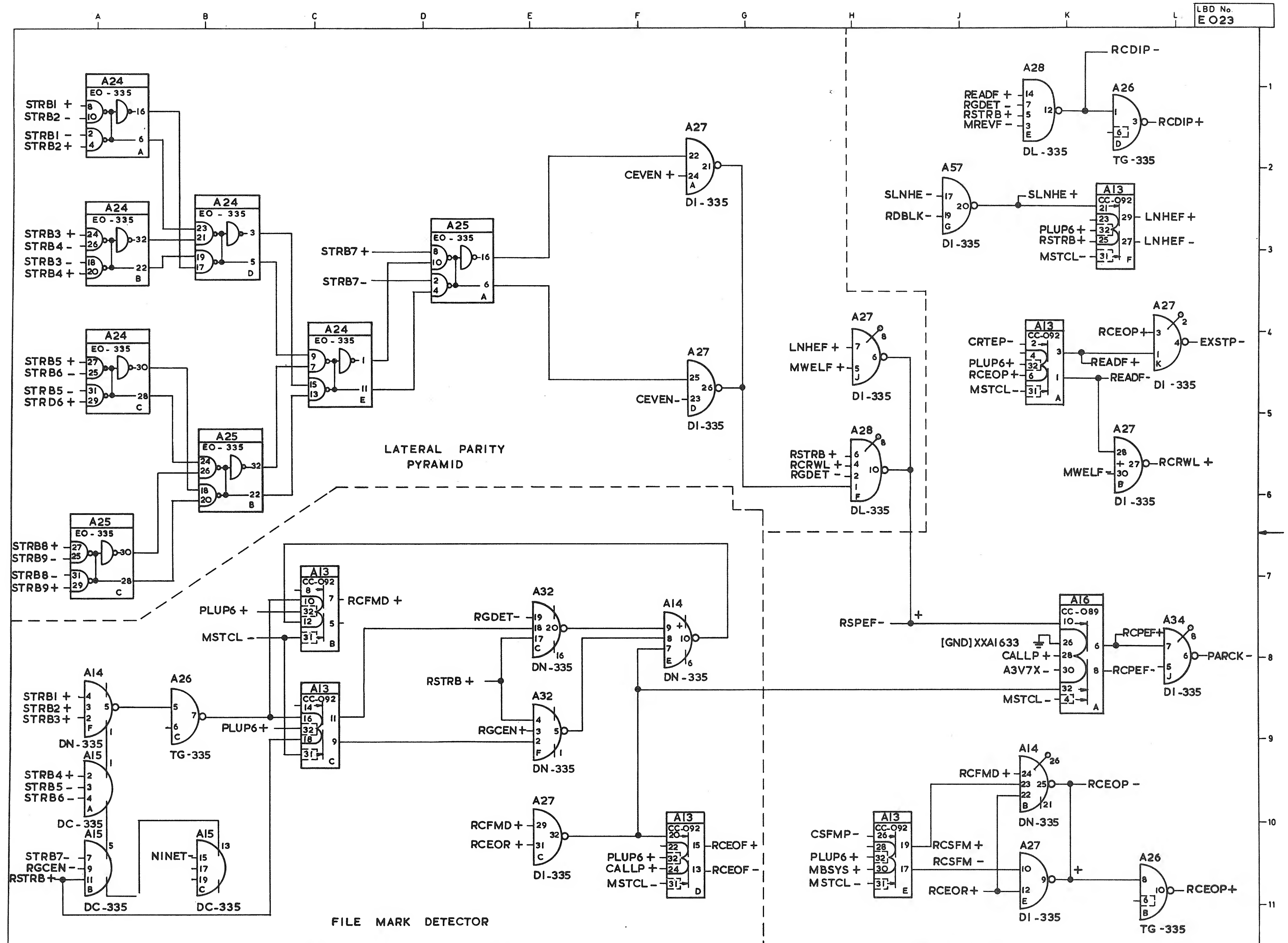
DR	DATE
ENG.	
APP	
PROJECT No	

TITLE
INPUT DATA CHARACTER
TAPE CONTROL UNIT
SERIES 16−4110

SIZE C | DWG No. FROM D42503007 SHT. 13 OF 23 | REV

3642/111

LBD No E023



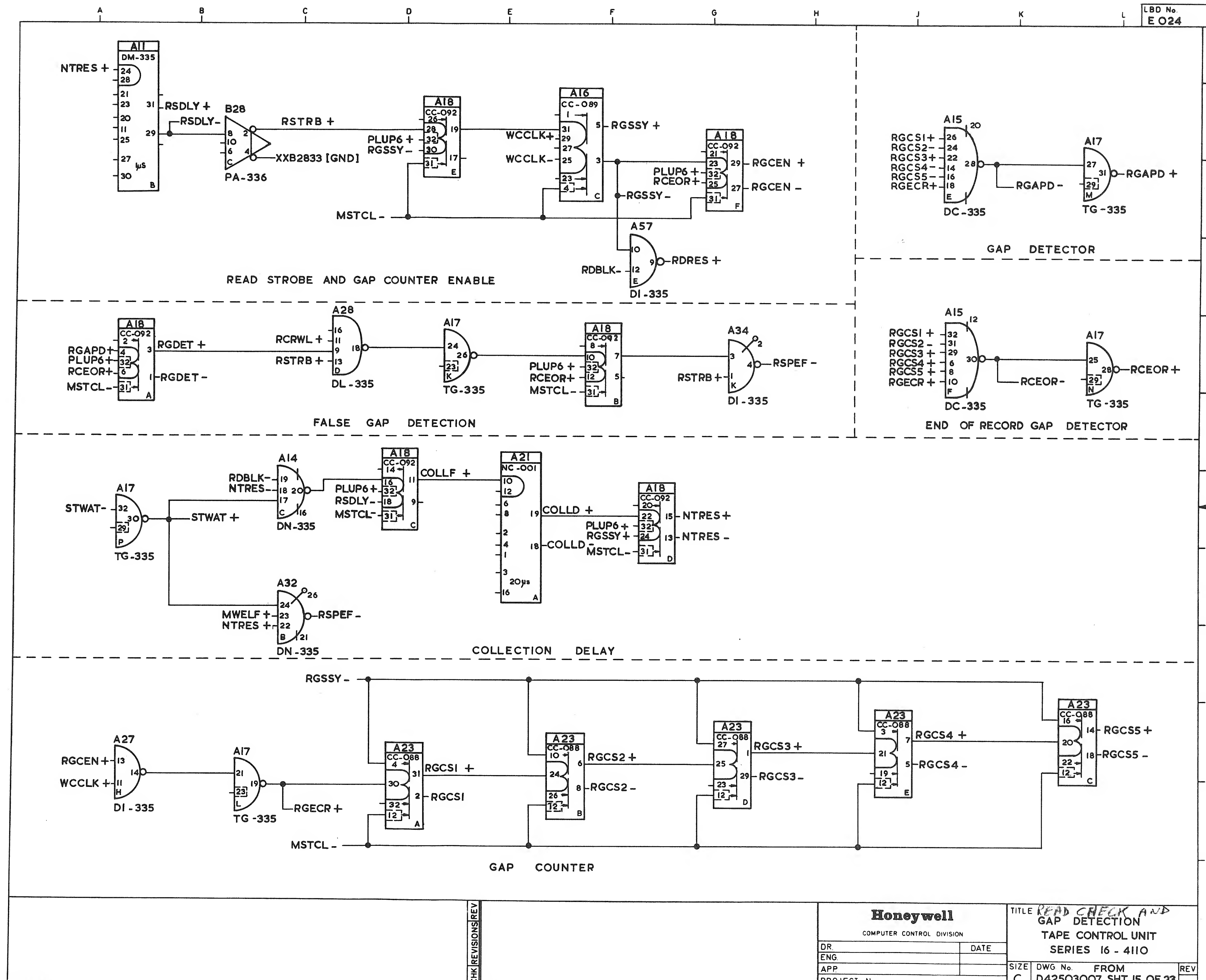
CHK	REVISIONS	REV

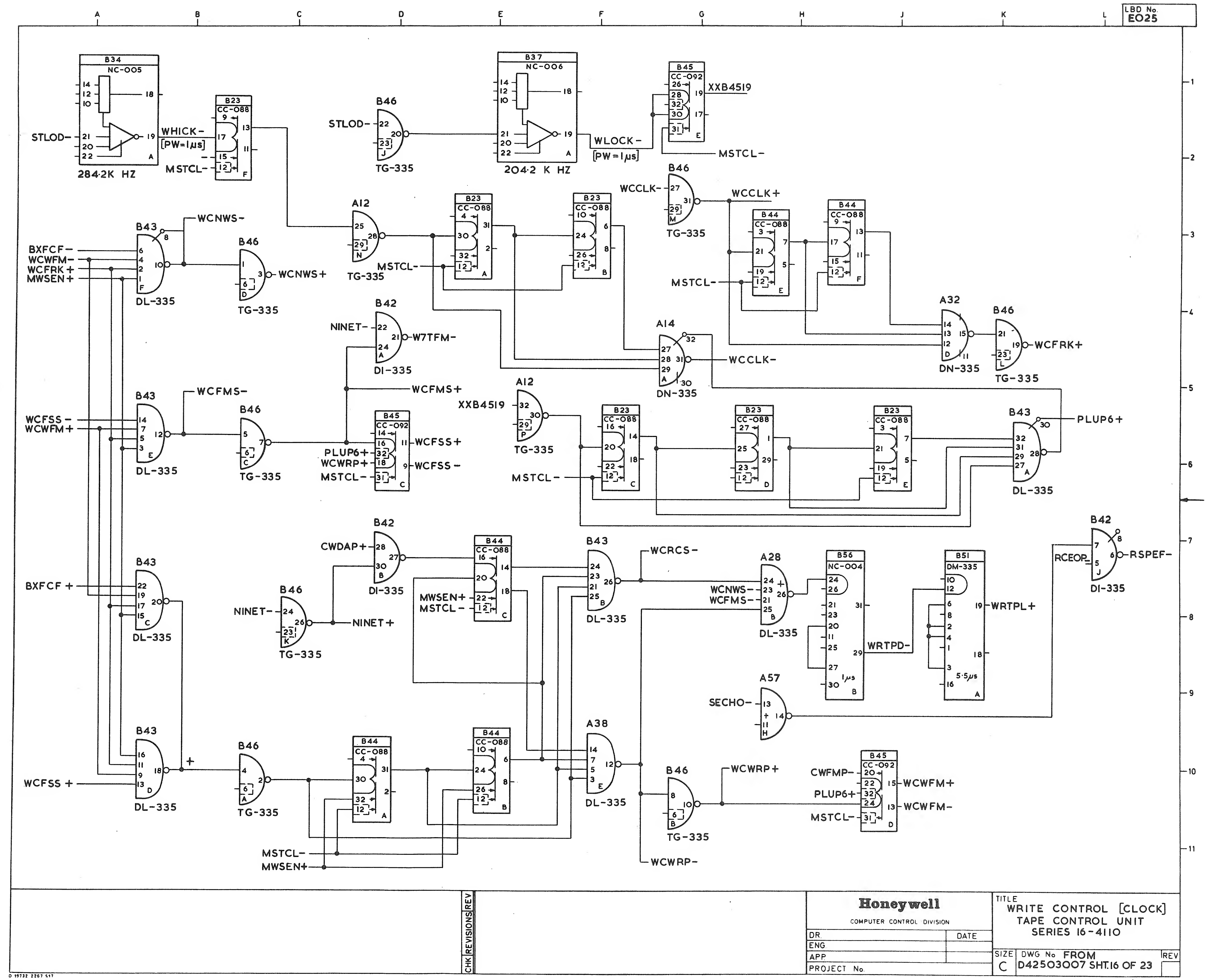
Honeywell
COMPUTER CONTROL DIVISION

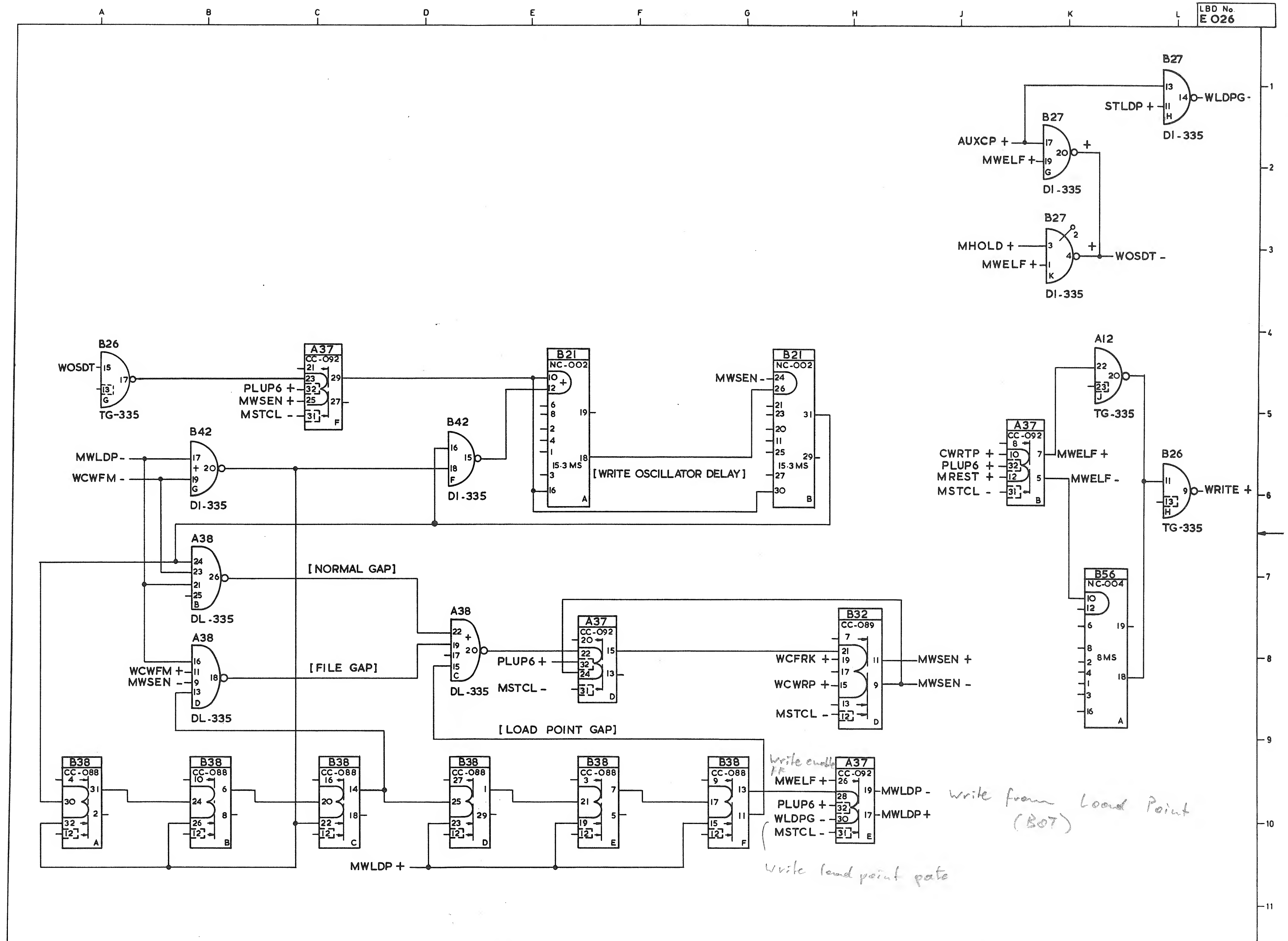
DR	DATE
ENG	
APP	
PROJECT No.	

TITLE
READ CONTROL
TAPE CONTROL UNIT
SERIES 16 - 4110

SIZE	DWG No	REV
C	FROM D42503007 SHEET 14 OF 23	

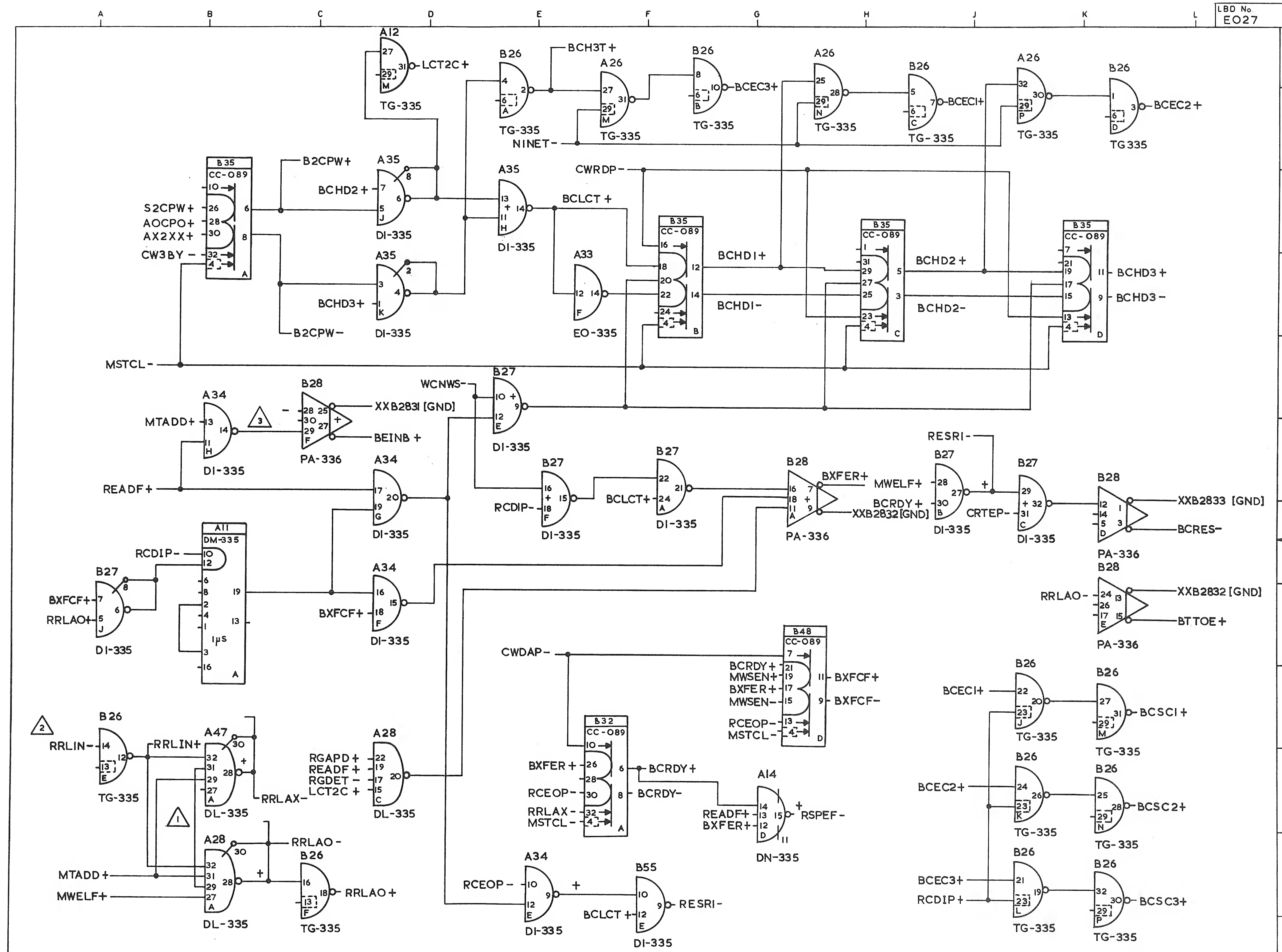

LBD No. E024
READ STROBE AND GAP COUNTER ENABLE
NTRES +
A11 DM-335
RSDLY +
RSDLY -
B28
PA-336
RSTRB +
XXB2833 [GND]
A18 CC-092
PLUP6 +
RGSSY -
A16 CC-089
WCCLK+
WCCLK-
RGSSY +
RGCEN +
RGCEN -
RCEOR+
RGSSY -
MSTCL -
A57
RDBLK-
RDRES +
DI-335
GAP DETECTOR
A15
RGCS1+
RGCS2-
RGCS3+
RGCS4-
RGCS5-
RGECR+
DC-335
RGAPD -
A17
RGAPD +
TG-335
FALSE GAP DETECTION
RGAPD+
RCEOR+
MSTCL-
RGDET +
RGDET -
A28
RCRWL +
RSTRB +
DL-335
A34
RSPEF -
END OF RECORD GAP DETECTOR
RCEOR-
RCEOR+
COLLECTION DELAY
STWAT-
STWAT +
A14
RDBLK-
NTRES-
DN-335
COLLF +
RSDLY-
A21 NC-001
20µs
COLLD +
COLLD -
NTRES+
NTRES -
A32
MWELF +
NTRES +
RSPEF -
GAP COUNTER
RGSSY -
A27
RGCEN+
WCCLK +
RGECR+
A23 CC-088
RGCS1 +
RGCS1
RGCS2 +
RGCS2 -
RGCS3 +
RGCS3 -
RGCS4 +
RGCS4 -
RGCS5 +
RGCS5 -
MSTCL -
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR.
DATE
ENG.
APP
PROJECT No.
TITLE READ CHECK AND GAP DETECTION
TAPE CONTROL UNIT
SERIES 16 - 4110
SIZE C
DWG No. D42503007
FROM SHT. 15 OF 23
REV


LBD No. E025
B34 NC-005
STLOD-
284.2K HZ
B23 CC-088
WHICK-
[PW=1μs]
MSTCL-
B46
STLOD-
TG-335
B37 NC-006
204.2 K HZ
WLOCK-
[PW=1μs]
B45 CC-092
XXB4519
MSTCL-
B46
WCCLK-
WCCLK+
TG-335
B44 CC-088
MSTCL-
A12
TG-335
B23 CC-088
MSTCL-
B43
WCNWS-
BXFCF-
WCWFM-
WCFRK+
MWSEN+
DL-335
B46
WCNWS+
TG-335
B42
NINET-
W7TFM-
DI-335
A14
WCCLK-
DN-335
A32
DN-335
B46
WCFRK+
TG-335
B43
WCFMS-
WCFSS-
WCWFM+
DL-335
B46
TG-335
WCFMS+
B45 CC-092
PLUP6+
WCWRP+
MSTCL-
WCFSS+
WCFSS-
A12
XXB4519
TG-335
MSTCL-
B43
PLUP6+
DL-335
B42
CWDAP+
DI-335
B46
NINET-
NINET+
TG-335
B44 CC-088
MWSEN+
MSTCL-
B43
WCRCS-
DL-335
A28
WCNWS-
WCFMS-
DL-335
B56 NC-004
WRTPD-
B51 DM-335
WRTPL+
5.5μs
B42
RCEOP
RSPEF-
DI-335
B43
BXFCF+
DL-335
A57
SECHO-
B43
WCFSS+
DL-335
B46
TG-335
B44 CC-088
A38
DL-335
B46
WCWRP+
TG-335
B45 CC-092
CWFMP-
PLUP6+
MSTCL-
WCWFM+
WCWFM-
MSTCL-
MWSEN+
WCWRP-
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR
DATE
ENG
APP
PROJECT No.
TITLE
WRITE CONTROL [CLOCK]
TAPE CONTROL UNIT
SERIES 16-4110
SIZE C
DWG No. FROM D42503007 SHT.16 OF 23
REV



Honeywell COMPUTER CONTROL DIVISION	TITLE WRITE CONTROL [GAP] TAPE CONTROL UNIT SERIES 16 - 4110
DR / ENG / APP / PROJECT No / DATE	SIZE C — DWG No FROM D42503007 SHT.17 OF 23 — REV

CHK REVISIONS REV



1. CONNECT A2829 TO A2833 FOR DMA OPTION 4108
2. WHEN DMA CONNECTIONS ARE MADE RRLIN- BECOMES OTPMA
3. REMOVE A3414 TO B2829 FOR DMA OPTION 4108

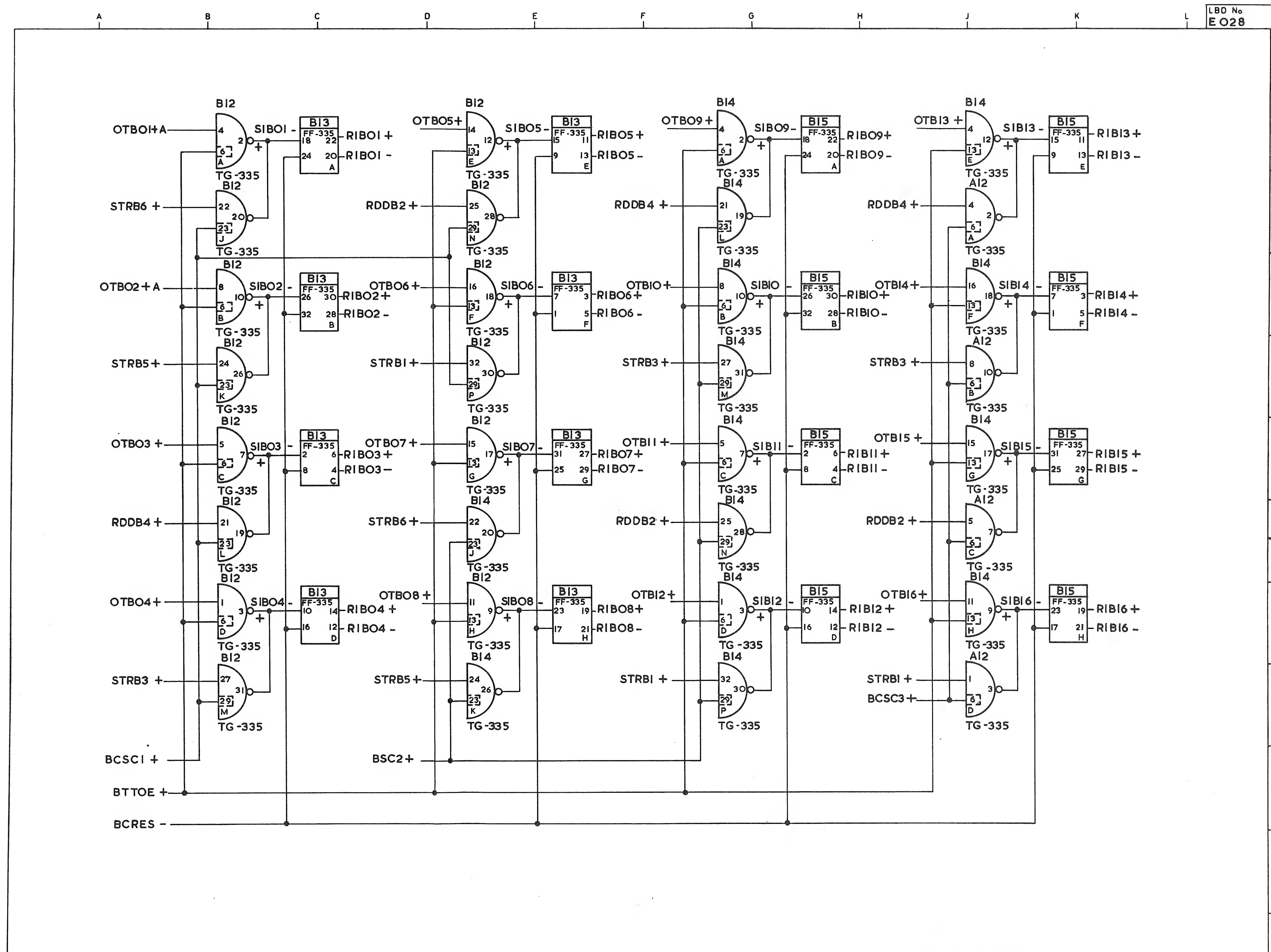
CHK REVISIONS REV

Honeywell
COMPUTER CONTROL DIVISION

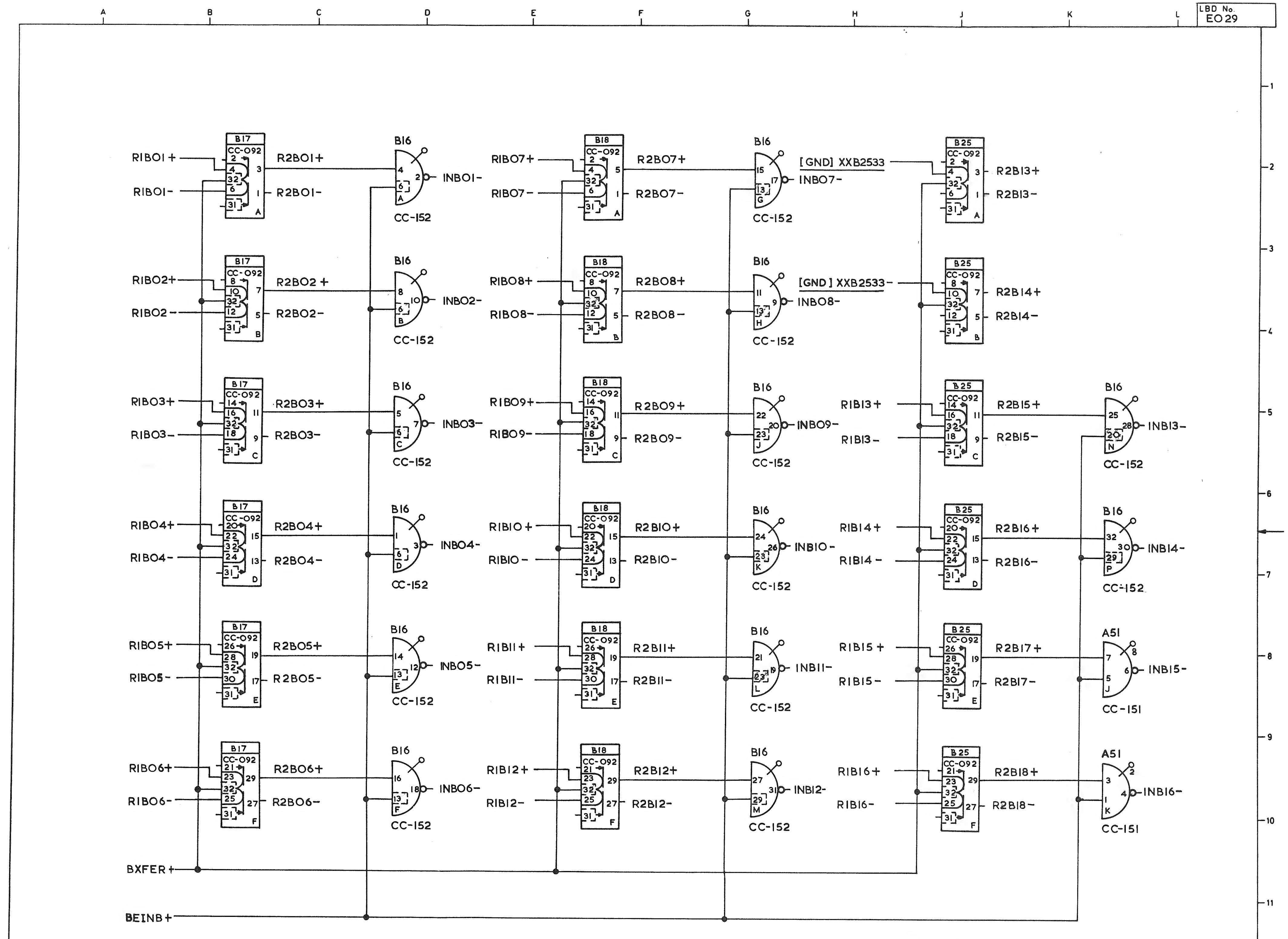
DR. | DATE
ENG.
APP.
PROJECT No.

TITLE
BUFFER CONTROL
TAPE CONTROL UNIT
SERIES 16 – 4110

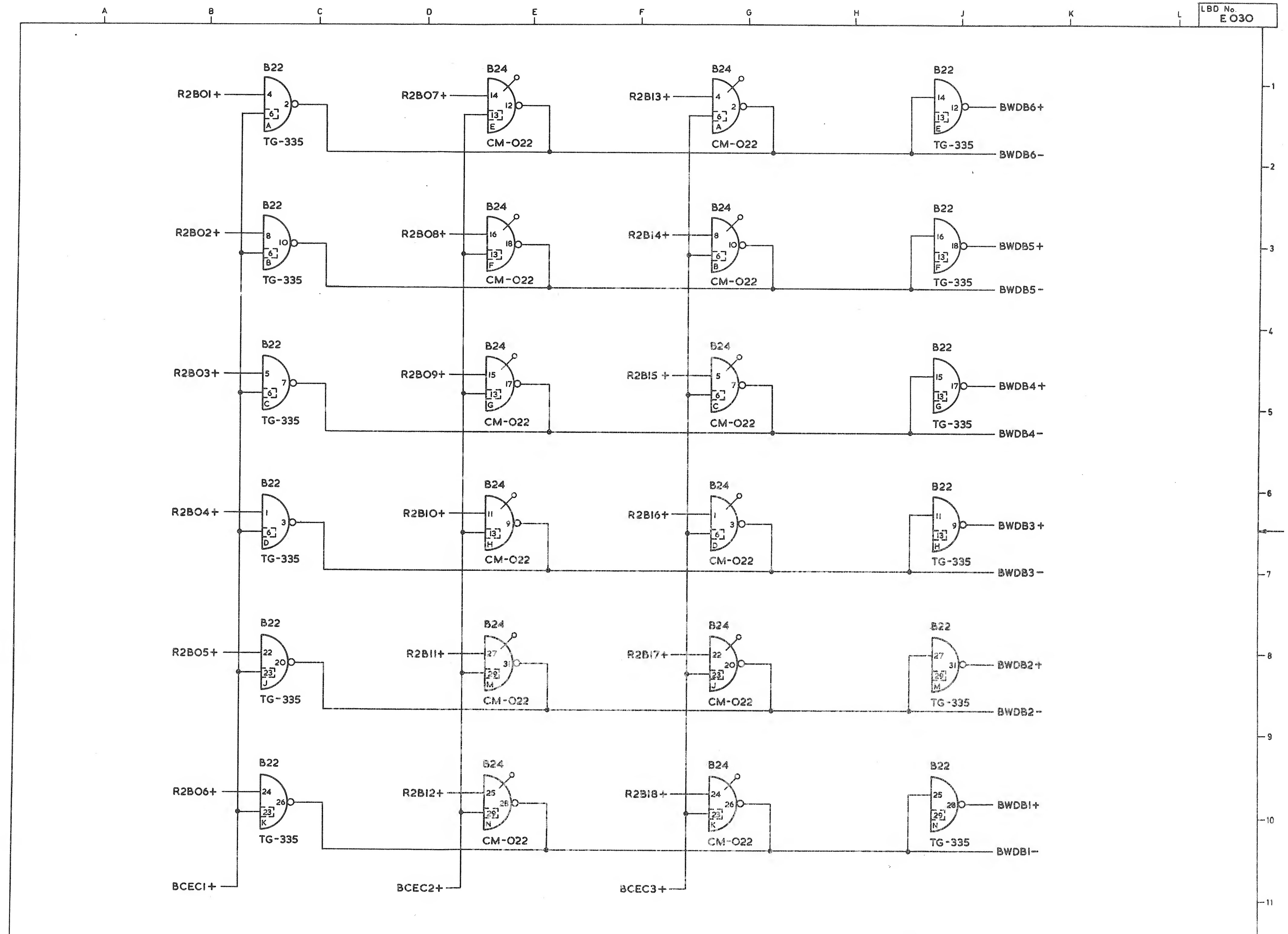
SIZE C DWG No D42503007 FROM SHT. 18 OF 23 REV



Honeywell COMPUTER CONTROL DIVISION	TITLE WORD BUFFER RANK 1 TAPE CONTROL UNIT SERIES 16-4110
DR / DATE / ENG / APP / PROJECT No.	SIZE C DWG. No. FROM D42503007 SHT.19 OF 23 REV



CHK REVISIONS REV	**Honeywell** COMPUTER CONTROL DIVISION	TITLE WORD BUFFER RANK 2 TAPE CONTROL UNIT SERIES 16- 4110
	DR. DATE / ENG. / APP. / PROJECT No.	SIZE C DWG No. D42503007 FROM SHT. 20 OF 23 REV



CHK | REVISIONS | REV

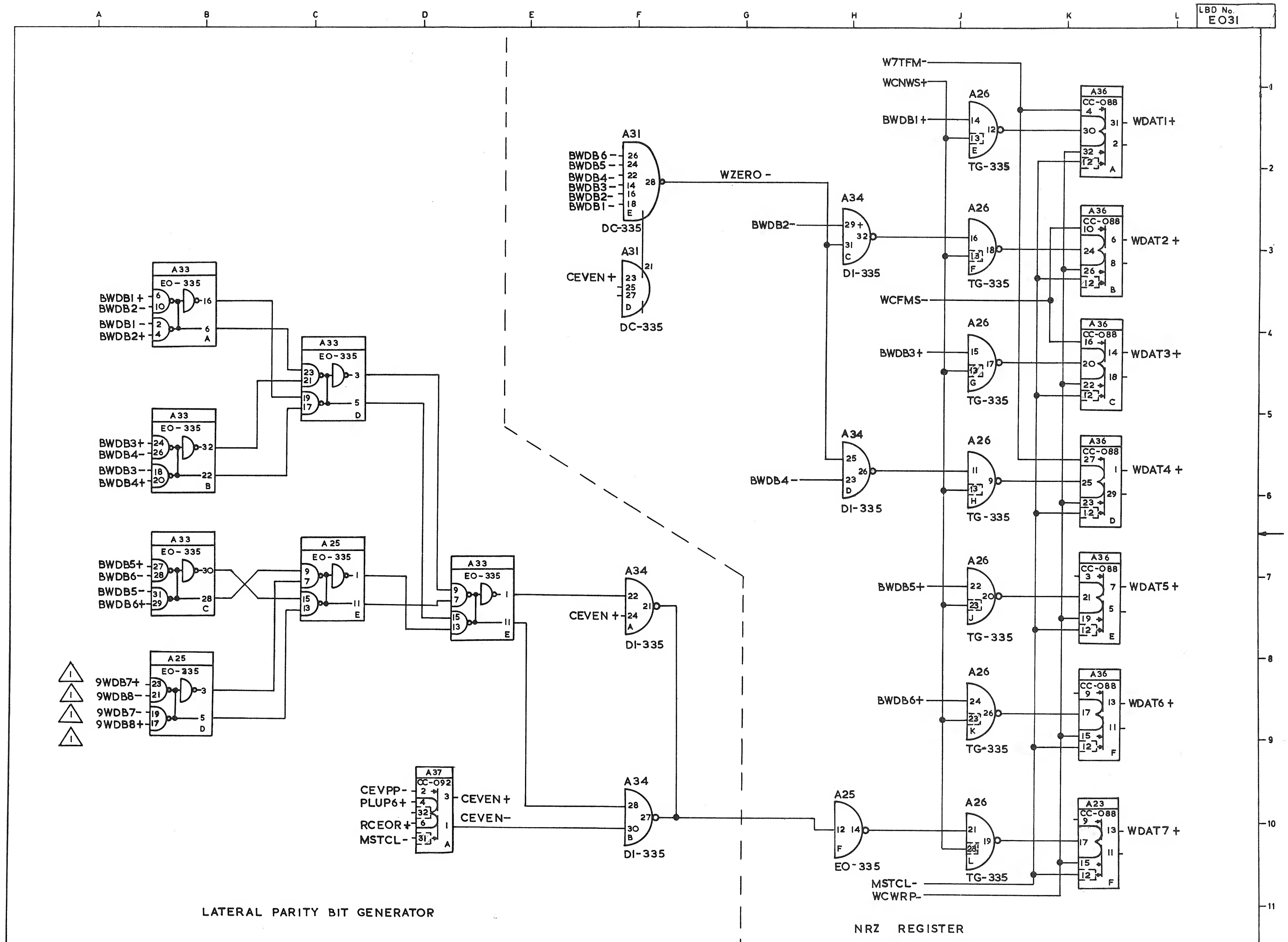
Honeywell
COMPUTER CONTROL DIVISION

DR | DATE
ENG
APP
PROJECT No

TITLE
OUTPUT DATA FORMATTING
TAPE CONTROL UNIT
SERIES 16 – 4110

SIZE C | DWG No D42503007 | FROM SHT.21 OF 23 | REV

MB 3642/82



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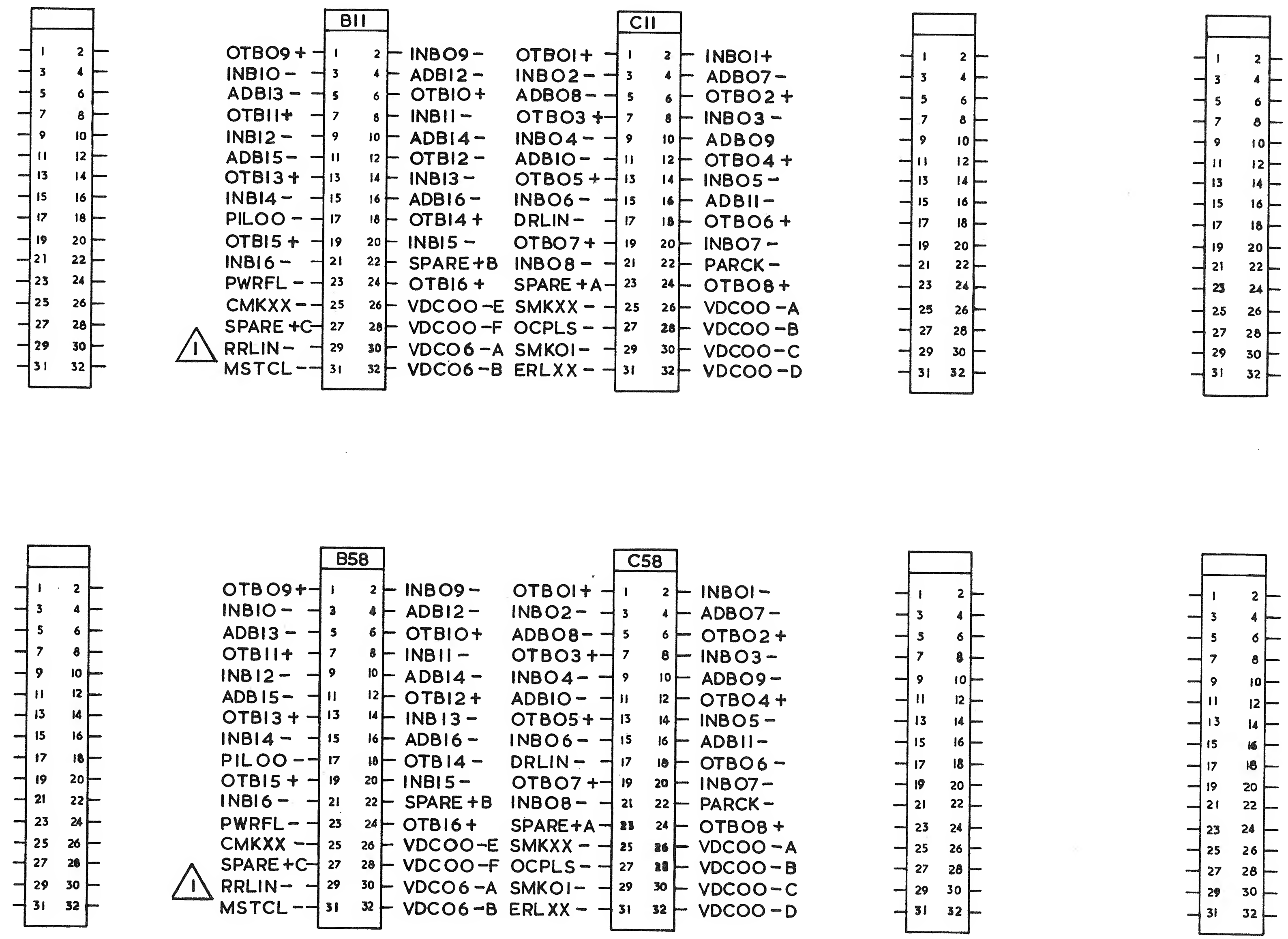
PROJECT No.	

TITLE
OUTPUT DATA CHARACTER
TAPE CONTROL UNIT
SERIES 16 — 4110

SIZE C DWG. No. FROM D42503007 SHT. 22 OF 23 REV

LBD No E032



NOTE

1. WHEN DMA CONNECTIONS ARE MADE RRLIN- BECOMES OTPMA-

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TITLE I/O CONNECTORS TAPE CONTROL UNIT SERIES 16 4110

SIZE C DWG No FROM D42503007 SHT 23 REV

LBD No. E035

μ-PAC xA	Signal	5JKVO UPA7D SIG	GND
1	TxFWD−	11	21
2	TxRWD+	12	A2
3	TxHIP−	13	A4
4	TxHRT−	14	24
5	TxPER+	15	B2
6	TxPRT−	16	B4
7	TxWPE+	17	27
8	TxADI−	18	C2
9	TxWC9−	19	C4
10	TxREV−	22	A1
11	TxRRS−	23	A3
12	TxWRP+	25	B1
13	TxADC−	26	B3
14	TxADO−	28	C1
15	TxAD2−	29	C3
16	TxWC8−	31	D2
17	TxWC7−	32	D4
18	TxWC5−	34	E2
19	TxWC4−	35	E4
20	TxWC2−	37	39
21	TxWC1−	38	F3
22	TxAD3−	41	D1
23	TxAD4−	42	D3
24	TxWC6−	43	33
25	TxAD5−	44	E1
26	TxAD6−	45	E3
27	TxAD7−	46	36
28	TxWC3−	47	F1
29	[SPARE]	48	F2
30	Tx15V+	49	F4
31			
32			

μ-PAC xB	Signal	5JKVO UPA3B SIG	GND
1	TxHID−	11	21
2	TxLOD−	12	A2
3	TxWTG−	13	A4
4	[SPARE]	14	24
5	TxRDG−	15	B2
6	Tx2LO+	16	B4
7	Tx3LO+	17	27
8	TxERG+	18	C2
9	Tx6LO+	19	C4
10	TxDYC−	22	A1
11	[SPARE]	23	A3
12	TxLNH+	25	B1
13	Tx1LO+	26	B3
14	Tx4LO+	28	C1
15	Tx5LO+	29	C3
16	Tx8LO+	31	D2
17	Tx9LO+	32	D4
18	Tx3HI+	34	E2
19	Tx4HI+	35	E4
20	Tx7HI+	37	39
21	Tx8HI+	38	F3
22	Tx7LO+	41	D1
23	TxBOT+	42	D3
24	Tx1HI+	43	33
25	Tx2HI+	44	E1
26	TxEOT+	45	E3
27	Tx5HI+	46	36
28	Tx6HI+	47	F1
29	Tx9HI+	48	F2
30	TxWAT+	49	F4
31			
32			

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PROJECT No.

TITLE
TCU/MTT CABLE
TAPE CONTROL UNIT
SERIES 16 4110

SIZE C | DWG. No. FROM D42503008 SHT. 1 | REV

LBD No. E036

LOCATION	FIRST UNIT AA	FIRST UNIT AB	SECOND UNIT BA	SECOND UNIT BB
	C18	C21	C28	C31
1	TAFWD−	TAHID−	TBFWD−	TBHID−
2	TARWD+	TALOD−	TBRWD+	TBLOD−
3	TAHIP−	TAWTG−	TBHIP−	TBWTG−
4	TAHRT−	[SPARE]	TBHRT−	[SPARE]
5	TAPER+	TARDG−	TBPER+	TBRDG−
6	TAPRT−	TA2LO+	TBPRT−	TB2LO+
7	TAWPE−	TA3LO+	TBWPE−	TB3LO+
8	TAADI−	TAERG−	TBADI−	TBERG−
9	TAWC9−	TA6LO+	TBWC9−	TB6LO+
10	TAREV−	TADYC−	TBREV−	TBDYC−
11	TARRS−	[SPARE]	TBRRS−	[SPARE]
12	TAWRP+	TALNH+	TBWRP+	TBLNH+
13	TAADC−	TAILO+	TBADC−	TBILO+
14	TAADO−	TA4LO+	TBADO−	TB4LO+
15	TAAD2−	TA5LO+	TBAD2−	TB5LO+
16	TAWC8−	TA8LO+	TBWC8−	TB8LO+
17	TAWC7−	TA9LO+	TBWC7−	TB9LO+
18	TAWC5−	TA3HI+	TBWC5−	TB3HI+
19	TAWC4−	TA4HI+	TBWC4−	TB4HI+
20	TAWC2−	TA7HI+	TBWC2−	TB7HI+
21	TAWCI−	TA8HI+	TBWCI−	TB8HI+
22	TAAD3	TA7LO+	TBAD3−	TB7LO+
23	TAAD4−	TABOT+	TBAD4−	TBBOT+
24	TAWC6−	TAIHI+	TBWC6−	TBIHI+
25	TAAD5−	TA2HI+	TBAD5−	TB2HI+
26	TAAD6−	TAEOT+	TBAD6−	TBEOT+
27	TAAD7−	TA5HI+	TBAD7−	TB5HI+
28	TAWC3−	TA6HI+	TBWC3−	TB6HI+
29	[SPARE]	TA9HI+	[SPARE]	TB9HI+
30	TAI5V+	TAWAT+	TBI5V+	TBWAT+
31				
32				
33				
34				

LOCATION	THIRD UNIT CA	THIRD UNIT CB	FOURTH UNIT DA	FOURTH UNIT DB
	C38	C41	C48	C51
1	TCFWD−	TCHID−	TDFWD−	TDHID−
2	TCRWD+	TCLOD−	TDRWD+	TDLOD−
3	TCHIP−	TCWTG−	TDHIP−	TDWTG−
4	TCHRT−	[SPARE]	TDHRT−	[SPARE]
5	TCPER+	TCRDG−	TDPER+	TDRDG−
6	TCPRT−	TC2LO+	TDPRT−	TD2LO+
7	TCWPE+	TC3LO+	TDWPE+	TD3LO+
8	TCADI−	TCERG−	TDADI−	TDERG−
9	TCWC9−	TC6LO+	TDWC9−	TD6LO+
10	TCREV−	TCDYC−	TDREV−	TDDYC−
11	TCRRS−	[SPARE]	TDRRS−	[SPARE]
12	TCWRP+	TCLNH+	TDWRP+	TDLNH+
13	TCADC−	TCILO+	TDADC−	TDILO+
14	TCADO−	TC4LO+	TDADO−	TD4LO+
15	TCAD2−	TC5LO+	TDAD2−	TD5LO+
16	TCWC8−	TC8LO+	TDWC8−	TD8LO+
17	TCWC7−	TC9LO+	TDWC7−	TD9LO+
18	TCWC5−	TC3HI+	TDWC5−	TD3HI+
19	TCWC4−	TC4HI+	TDWC4−	TD4HI+
20	TCWC2−	TC7HI+	TDWC2−	TD7HI+
21	TCWCI−	TC8HI+	TDWCI−	TD8HI+
22	TCAD3−	TC7LO+	TDAD3−	TD7LO+
23	TCAD4−	TCBOT+	TDAD4−	TDBOT+
24	TCWC6−	TCIHI+	TDWC6−	TDIHI+
25	TCAD5−	TC2HI+	TDAD5−	TD2HI+
26	TCAD6−	TCEOT+	TDAD6−	TDEOT+
27	TCAD7−	TC5HI+	TDAD7−	TD5HI+
28	TCWC3−	TC6HI+	TDWC3−	TD6HI+
29	[SPARE]	TC9HI+	[SPARE]	TD9HI+
30	TCI5V+	TCWAT+	TDI5V+	TDWAT+
31				
32				
33				
34				

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TCU/MTT CABLE
TAPE CONTROL UNIT
SERES 16 4110

SIZE C DWG No. FROM D42503008 SHT.2 REV

APPENDIX

PAC DESCRIPTIONS

This appendix contains descriptions of the following u-PAC's:-

Counter PAC, model CC-088

Gated flip-flop PAC, model CC-089

Buffer register PAC, model CC-092

Resistor PAC, model CC-130

Delay Multivibrator, model CC-138

Delay Multivibrator, model CC-139

NAND gate PAC, model CC-151

Transfer gate PAC, model CC-152

Six Volt Line Driver PAC, model CC-165

Parallel transfer gate PAC, model CM-022

Delay Multivibrator, model NC-001

Delay Multivibrator, model NC-002

Delay Multivibrator, model NC-003

Delay Multivibrator, model NC-004

Master Clock PAC, model NC-005

Master Clock PAC, model NC-006

COUNTER PAC, MODEL CC-088

The Counter PAC, Model CC-088 (Figures CC-088-1 and CC-088-2), contains six independent flip-flops that can be used for counting, frequency division, and buffer storage. Each stage has a complement input, dc set and dc reset inputs, and set and reset outputs. There is also a common reset input for clearing all stages simultaneously. Application of a signal to the complement input causes the flip-flop to change state. (Toggling action is accomplished without additional wiring.)

INPUT AND OUTPUT SIGNALS

DC Set and Reset

A signal at 0v for 80 ns or longer on the dc set (or reset) input will set (or reset) the flip-flop.

Common Reset

A signal at 0V for 80 ns or longer on the common reset input will clear the six counter stages simultaneoulsy.

Complement

The output changes state on the negative transition of the complement input. This input is the same as the clock input of the integrated circuit flip-flop.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 MHz

Input Loading

DC inputs:	2/2 unit load each
Common reset:	4 unit loads
Complement:	1 unit load each

Output Drive Capability

8 unit loads each

Power Dissipation

0.90 W (max)

Handle Colour Code

Blue

Circuit Delay

Complement input to flip-flop outputs (counter propagation stage delay): 60 ns (max)

DC set input to set output, or dc reset input to reset output: 80 ns (max)

DC set input to reset output, or reset input to set output: 60 ns (max)

Current Requirements

+6V : 150 mA (max)

APPLICATIONS

Each of the stages can be used separately for divide-by-two, complementing operation. Successively connecting the set output of one stage to the complement input of another stage results in frequency division by factors of 4, 8, 16, 32 or 64. In this configuration, the PAC has a capacity as a counter of 0 through $2^6 - 1$, a total of 64 states.

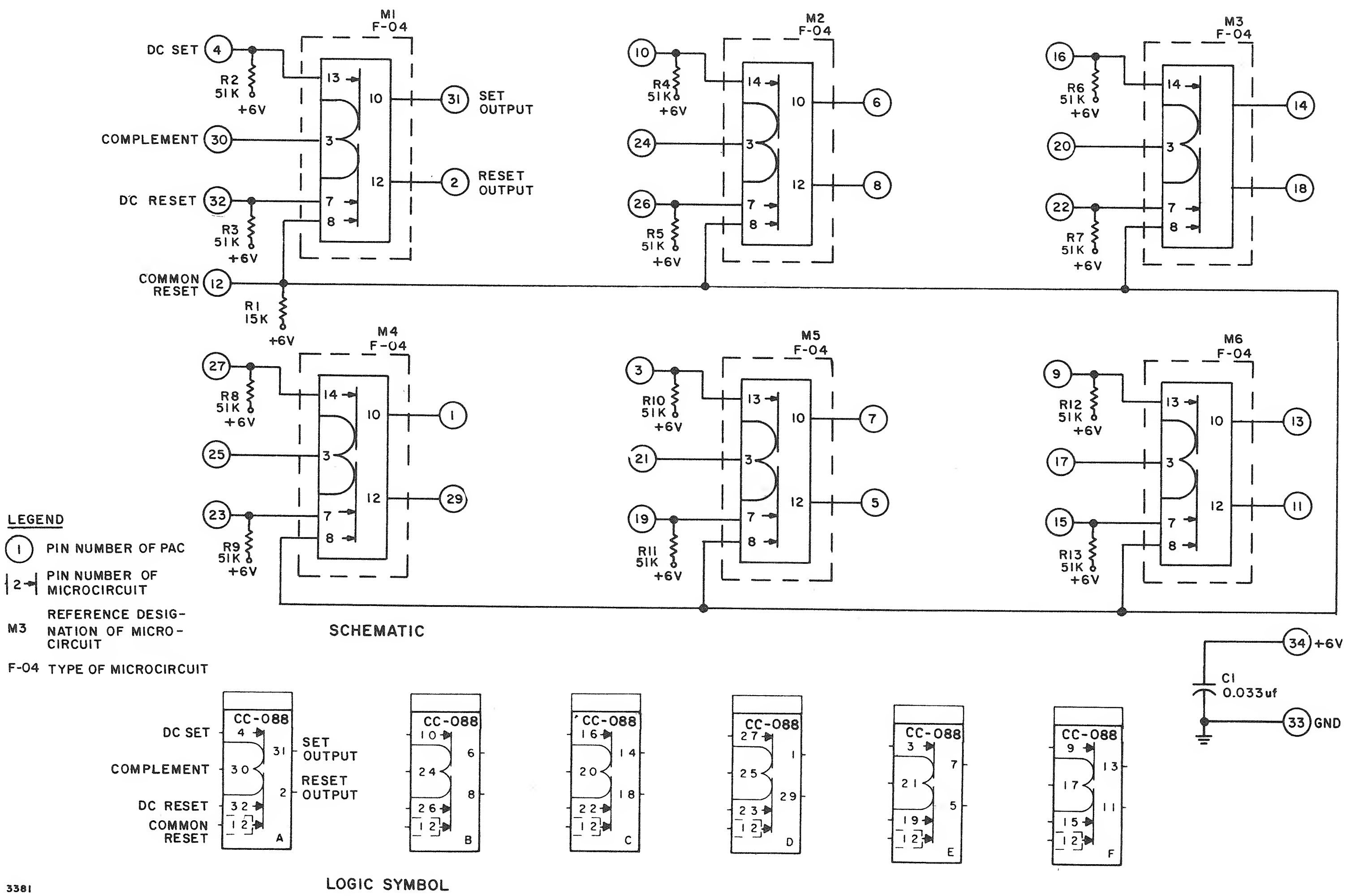

Figure CC-088-1 Counter PAC, Schematic Diagram and Logic Symbol

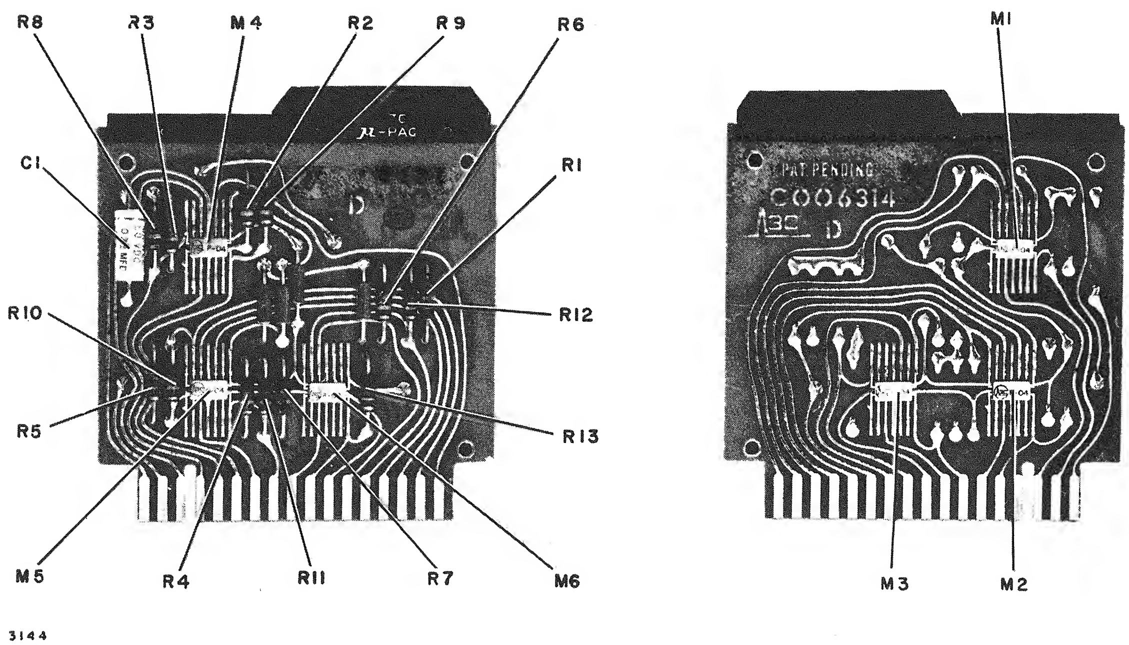

Figure CC 088-2 Counter PAC, Parts Location

Electrical Parts List

Ref. Designation	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033μF ±20%, 50 Vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15 K ±5%, 1/4 W	932 007 077
R2-R13	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4 W	932 007 090

GATED FLIP-FLOP PAC, MODEL CC-089

The Gated Flip-Flop PAC, Model CC-089 (Figures CC-089-1 and CC-089-2), contains four independent flip-flops. A versatile input structure allows control from a variety of levels and pulses. Typical applications are storage, counting and shifting, and control.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset

A signal at 0V for 80 ns or longer on a dc set (or reset) input will set (or reset) the flip-flop.

Common Reset

A signal at 0V for 80 ns or longer on the common reset input clears all four stages simultaneously.

Set Control and Reset Control

The enabling level on the control inputs is +6V.

Clock

The flip-flop changes state on the negative transition of the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 MHz

Input Loading

DC inputs:	2/2 unit load each
Control inputs:	1 unit load each
Common reset:	3 unit loads
Clock:	1 unit load each

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output:	60 ns (max)
DC set input to dc set output, or dc reset input to reset output:	80 ns (max)
DC set input to reset output, or dc reset input to set output:	60 ns (max)

Current Requirements

+6V: 100 mA (max)

Power Dissipation

0.60 W (max)

Handle Colour Code

Blue

APPLICATIONS

Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones. For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation.

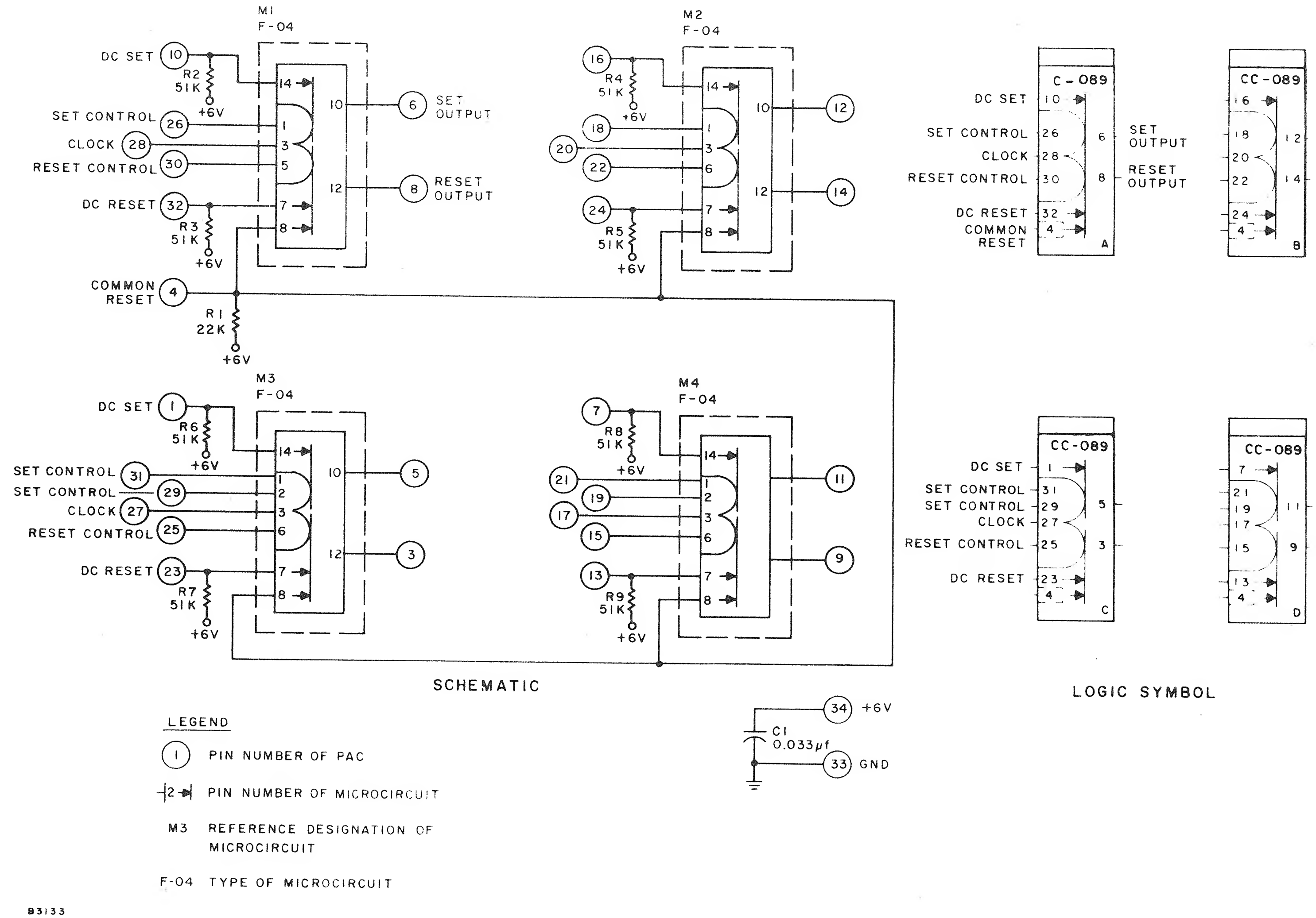

Figure CC-089-1. Gated Flip-Flop PAC, Schematic Diagram and Logic Symbol

Figure CC-089-1 Gated Flip-Flop PAC, Schematic Diagram and Logic Symbol

Figure CC-089-2   Gated Flip-Flop PAC, Parts Location

Electrical Parts List

Ref. Designation	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033μF ±20%, 50 Vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22 K ±5%, 1/4 W	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4 W	932 007 090

BUFFER REGISTER PAC, MODEL CC-092

The Buffer Register PAC, Model CC-092 (Figures CC-092-1 and CC-092-2), contains six flip-flops. Common clock and common reset inputs make simultaneous operations possible on all stages. Typical uses include shifting, accumulating, and clocked parallel transfer.

INPUT AND OUTPUT SIGNALS

DC Set

A signal at 0V for 80 ns or longer on dc set input will set the flip-flop.

Set Control and Reset Control

The enabling level on the control inputs is +6V.

Common Clock

The flip-flops change state on the negative transition of the clock input.

Common Reset

A signal at 0V for 80 ns or longer on the common reset input clears all the six stages simultaneously.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 MHz

Input Loading

DC set:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	4 unit loads
Common clock:	6 unit loads

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output: 60 ns (max)

DC set input to set output, or common reset input to reset output: 80 ns (max)

DC set input to reset output, or common reset input to set output: 60 ns (max)

Current Requirements

+6V: 150 mA (max)

Power Dissipation

0.90 W (max)

Handle Colour Code

Blue

APPLICATIONS

For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation. Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones.

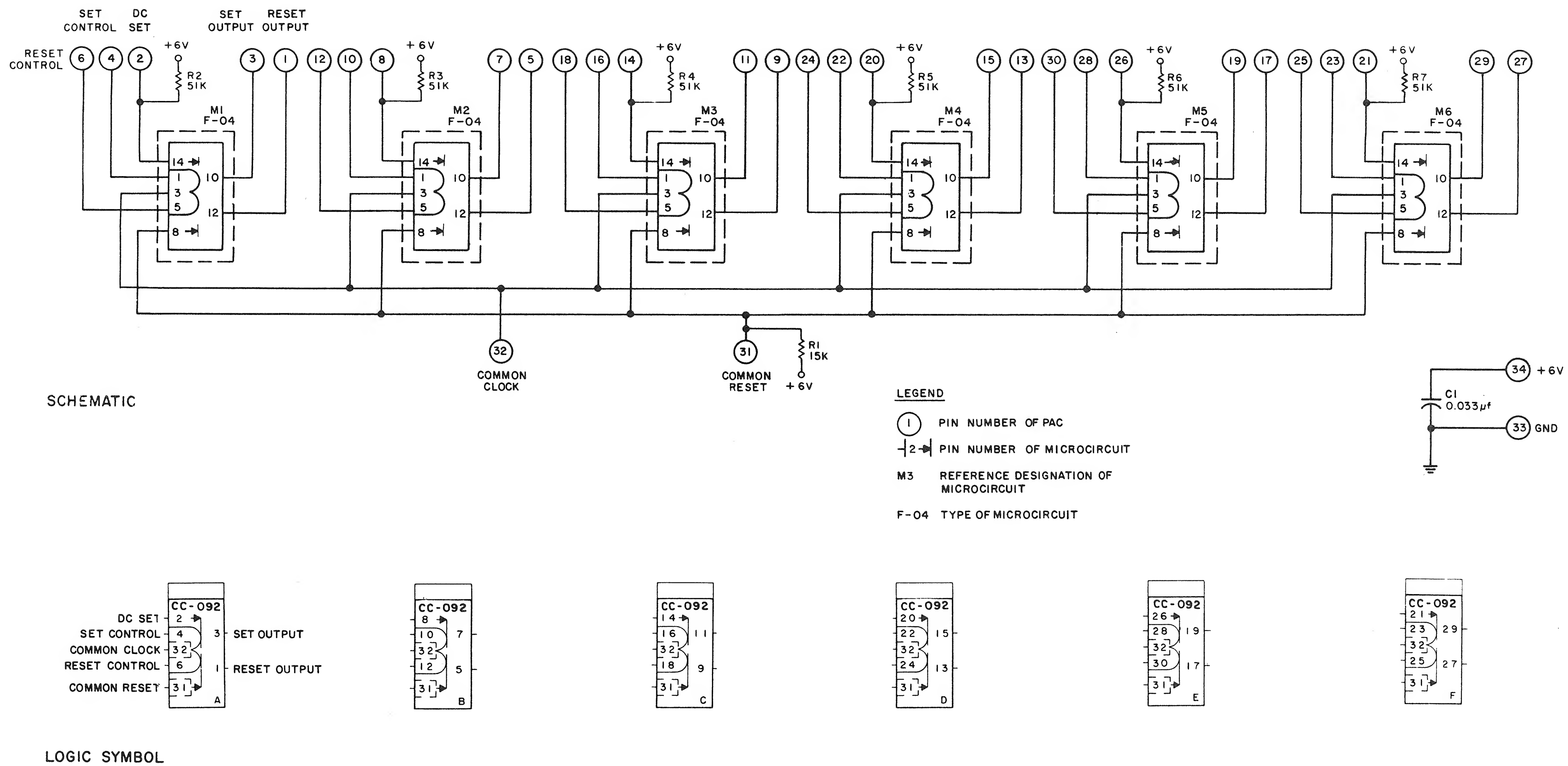

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Figure CC-092-1 Buffer Register PAC, Schematic Diagram and Logic Symbol

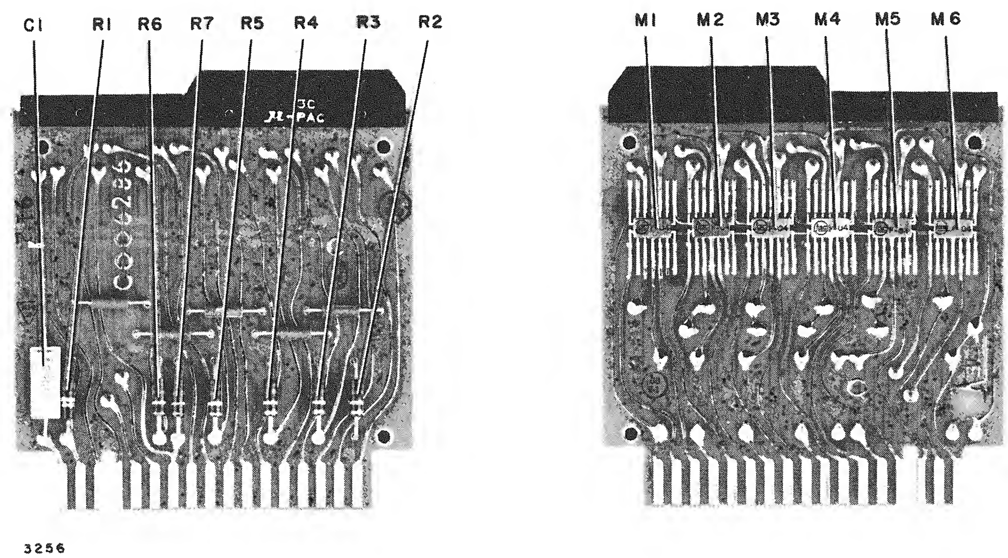


Figure CC-092-2 Buffer Register PAC, Parts Location

Electrical Parts List

Ref. Designation	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 uF $\pm$20%, 50 Vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15K $\pm$5%, 1/4 W	932 007 077
R2-R7	RESISTOR, FIXED, COMPOSITION: 51K $\pm$5%, 1/4 W	932 007 090

RESISTOR PAC, MODEL CC-130

The Resistor PAC, Model CC-130 (Figure 1), consists of 20 1K resistors. One end of each resistor is brought out to a separate PAC pin. The other ends of the resistors are connected to $+V_{cc}$ on the PAC.

NOTE

The following pins must be jumpered together as indicated:

Pins 2 to 18 to 33
Pins 5 to 15 to 33

Electrical Parts List

Ref. Designation	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µF ±20%, 50 Vdc	930 313 016
R1-R20	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	932 007 049

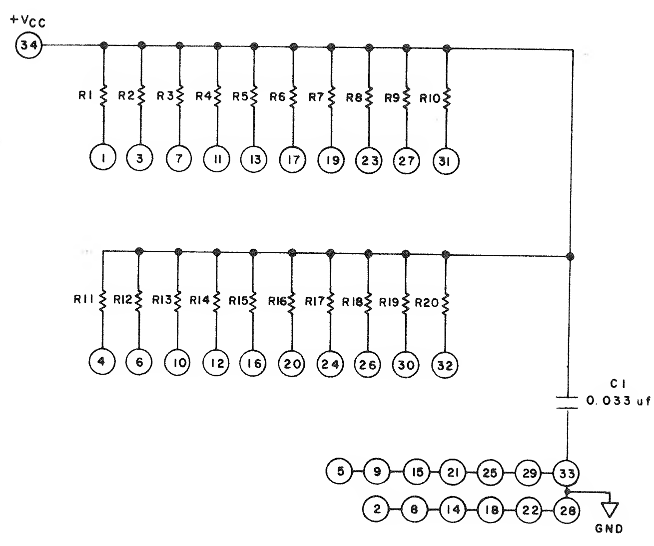


Figure CC-130-1 Resistor PAC, Schematic Diagram

DELAY MULTIVIBRATOR PAC, MODEL CC-138

The model CC-138 μ-PAC is identical to the DM-335 μ-PAC except as follows:-

C6:	CAPACITOR, FIXED, TANTALUM: 2.2 μF $\pm$5%, 10 Vdc	930 235 044
C11:	CAPACITOR, FIXED, TANTALUM: 0.47 μF $\pm$5%, 35 Vdc	930 235 040
R3:	RESISTOR, FIXED, FILM: 4.7K $\pm$2%, 1/4W	932 114 065
R7:	RESISTOR, FIXED, FILM: 5.6K $\pm$2%, 1/4W	932 114 067
Delay:	Circuit A 8 milli-seconds	
	Circuit B 2 milli-seconds	

DELAY MULTIVIBRATOR PAC, MODEL CC-139

The model CC-139 μ-PAC is identical to the DM-335 μ-PAC except as follows:-

C6, C11:	CAPACITOR, FIXED, TANTALUM: 22 μF $\pm$5%, 10 Vdc	930 235 015
R3, R7:	RESISTOR, FIXED, FILM: 3.6K $\pm$2%, 1/4W	932 114 062
Delay:	Both circuits 60 milli-seconds	

NAND GATE PAC, MODEL CC-151

GENERAL

The NAND Gate PAC, Model CC-151 (Figure 1), contains ten independent 2-input NAND gates. Two of the circuits (J and K) have Miller feedback capacitors to limit the turn-on rise time to a minimum of 50 nsec. These two circuits are also provided with separate load connections made available at the PAC terminals.

The operation of the two F-02 microcircuits (J and K) is described in Section II of the u-PAC Integrated Circuit Modules Instruction Manual, Doc. No. 130071369. The operation of the F-01 microcircuits is also as described in Doc. No. 130071369 except that the delay is longer because of the Miller capacitors.

SPECIFICATIONS

Frequency of Operation

DC to 5MHz(A through H)

DC to 1MHz (J, K)

Input Loading

1 unit load each

Output Drive

8 unit loads

Circuit Delay

Average over two states

150 nsec (J, K)
30 nsec (A through H)

Current Requirements

+6V 125 mA (max)

Power Dissipation

0.75 W (max)

Electrical Parts List

Ref. Designation	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF $\pm$20%, 50 Vdc	930 313 016
C2, C3	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 10 pF $\pm$10%, 100 Vdc	930 173 204
M1, M2	MICROCIRCUIT: F-02 quad NAND gate integrated circuit	950 100 002
M3	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001

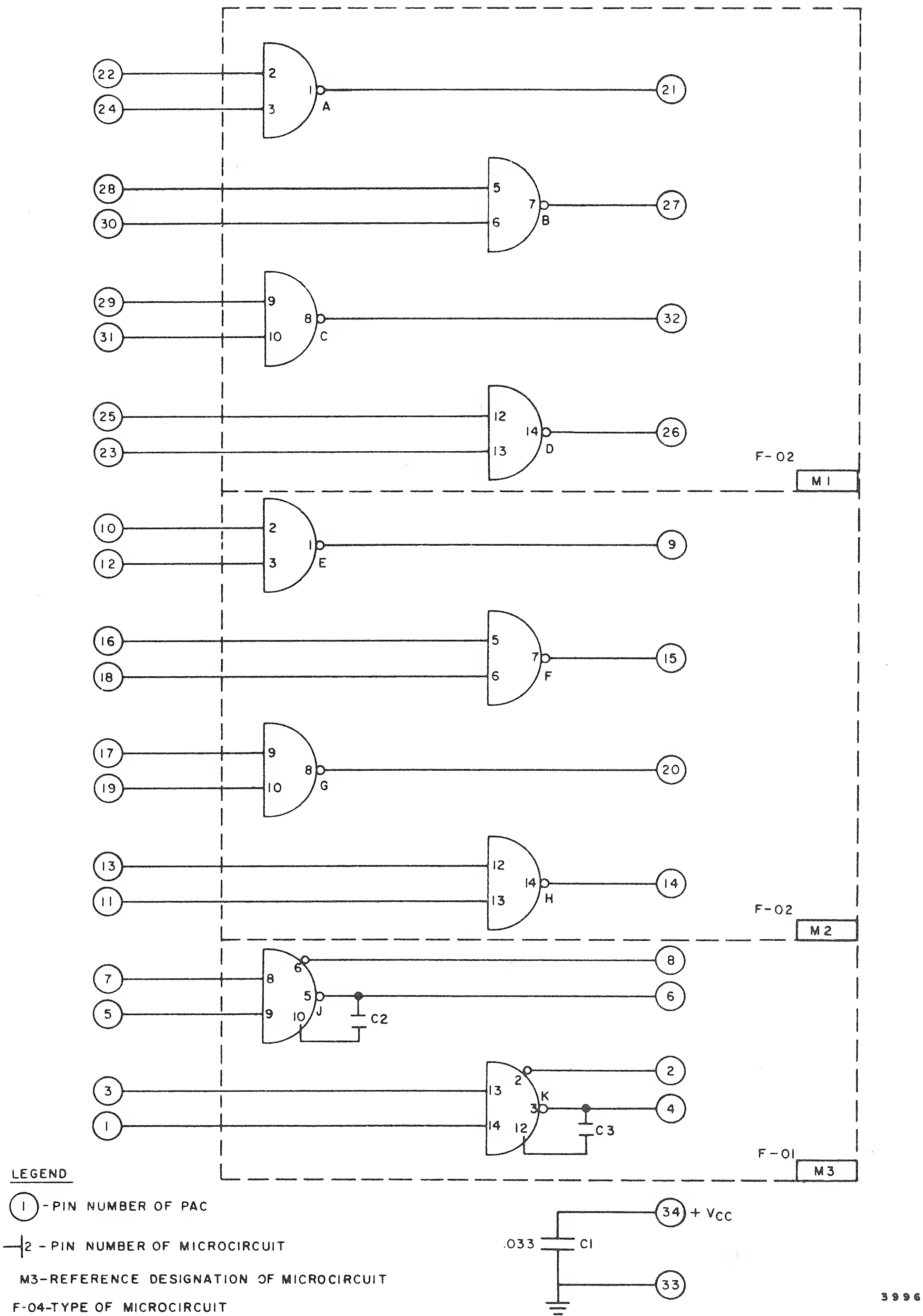


Figure CC-151-1 NAND Gate PAC, Schematic Diagram

TRANSFER GATE PAC, MODEL CC-152

GENERAL

The Transfer Gate PAC, Model CC-152 (Figure 1), contains 14 2-input NAND gates without collector resistors arranged in four independent groups. Two of the groups contain four NAND gates each with one input being common to the four gates. The other two groups contain three NAND gates each with one input being common to the three gates. All fourteen circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The Model CC-152 PAC can be used for the common transfer control of up to 14 data signals with the common input used as a control or strobe input. Turn-on rise time is controlled so as to have a guaranteed minimum of 50 nsec with no load.

SPECIFICATIONS

<u>Frequency of Operation</u>

DC to 5mHz(max)

<u>Input Loading</u>

Individual inputs:	1 unit load each
Common inputs:	1 unit load per gate

<u>Output Drive Capability</u>

8 unit loads

<u>Circuit Delay</u>

120 nsec (max) turn-on
40 nsec (max) turn-off

<u>Current Requirements</u>

+6V: 95 mA

<u>Power Dissipation</u>

560 mW (max)

Electrical Parts List

Ref. Designation	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016
C2-C15	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 10 pF ±10%, 100 Vdc	930 173 204
M1-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001

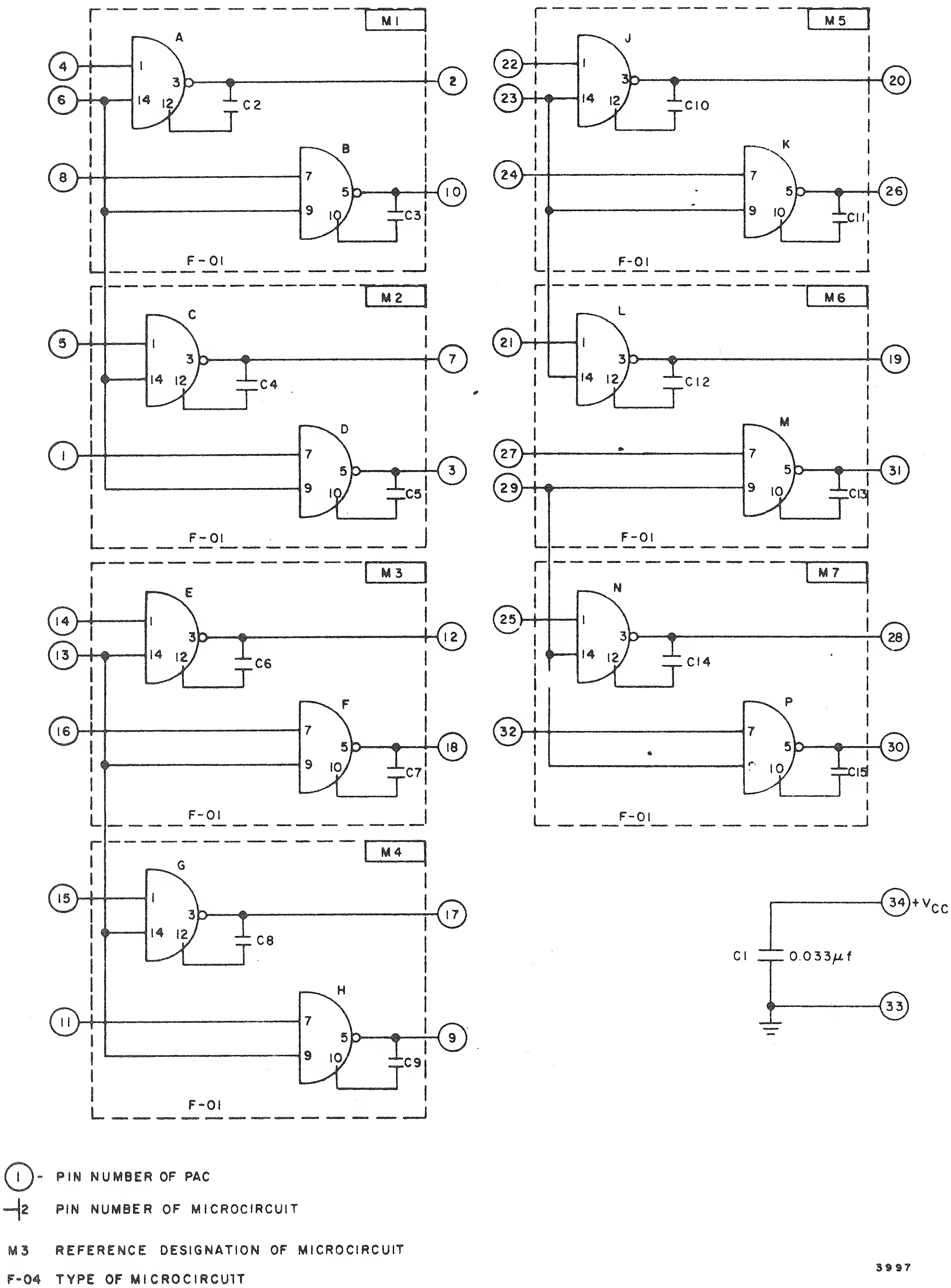


Figure CC-152-1 Transfer Gate PAC, Schematic Diagram

SIX VOLT LINE DRIVER PAC, MODEL CC-165

The Six Volt Line Driver PAC, Model CC-165 (Figure 1), contains six identical and independent circuits. Each circuit is capable of driving 62-ohm transmission line at +6 volt levels. Parts locations are illustrated in Figure 2.

CIRCUIT DESCRIPTION

Each of the six circuits operates, basically, as a clamp switch. When both inputs of each circuit are at a logic ONE, the transistor is turned on, clamping the output to ground through a 62-ohm resistor. When the inputs are at logic ZERO, the transistor is off, and the output is clamped to +6V through a 62-ohm resistor and diode. The transition time is slowed down by use of a capacitor so as to minimize crosstalk problems on the cable.

SPECIFICATIONS

Frequency of Operation

DC to 3kHz

Input Loading

1 unit load

Output Drive Capability

50 feet of 62-ohm cable and
2 unit loads

Circuit Delay

Turn-on: 650 ns (typ)

Turn-off: 210 ns (typ)

Current Requirements

+6V: 9 mA (max) into supply

+15V: 100 mA (max)

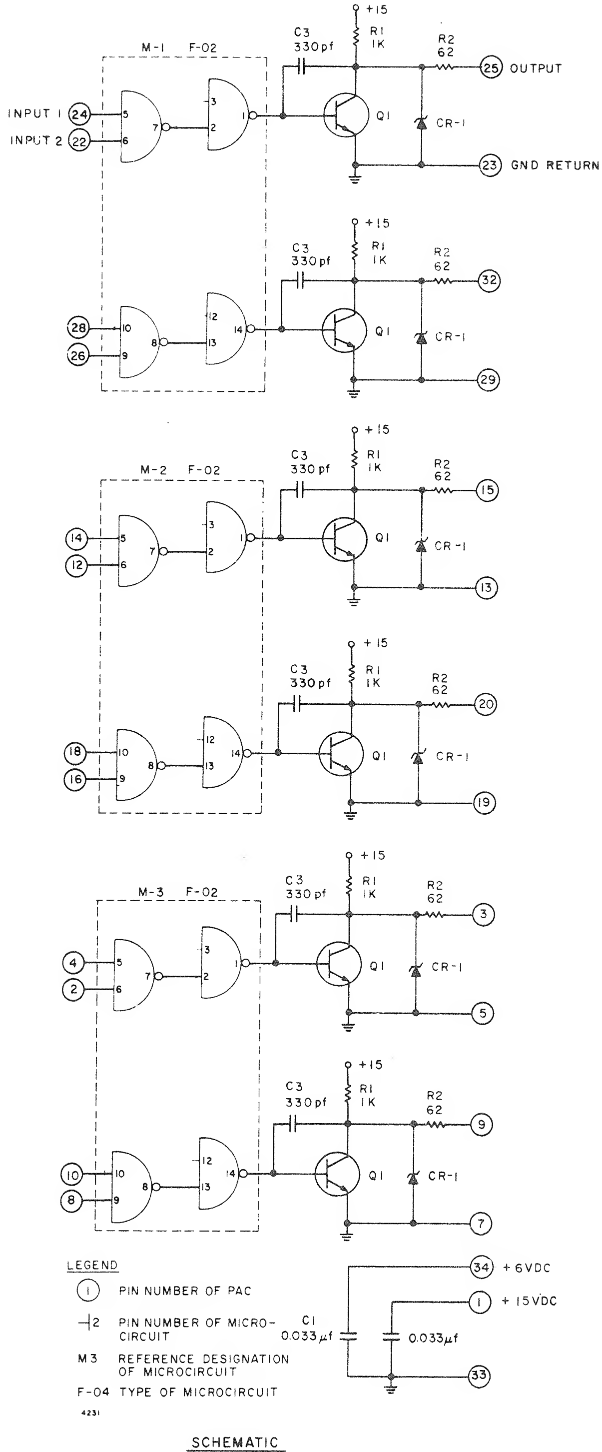
Power Dissipation

1.5 watts (max)

Output Timing

Rise Time: 700 ns (typ)

Fall Time: 600 ns (typ)



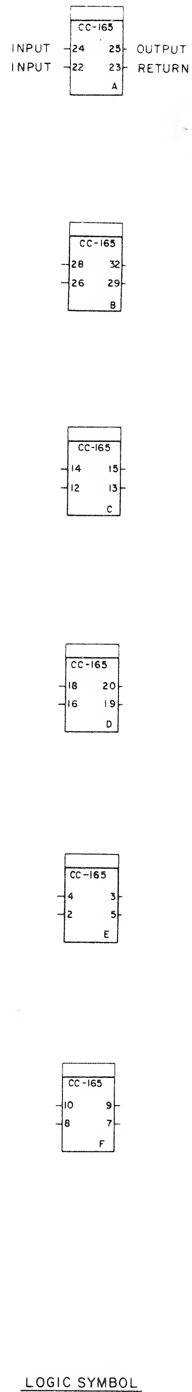


Figure CC-165-1 Line Driver PAC, Schematic Diagram and Logic Symbol

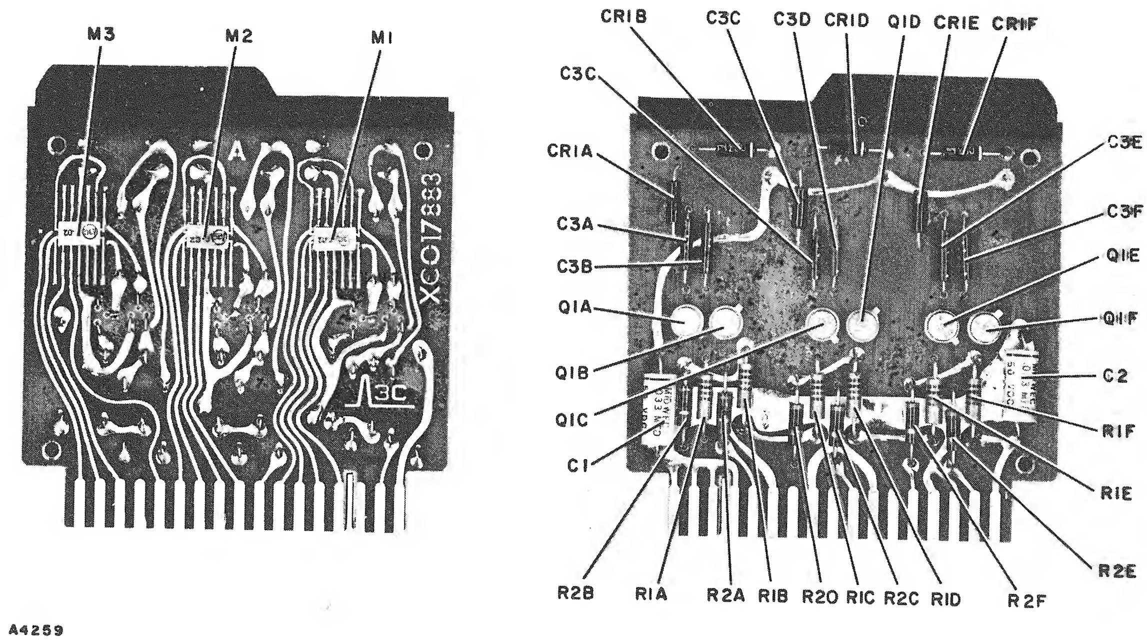


Figure CC-165-2 Line Driver PAC, Parts Location

Electrical Parts List

Ref. Designation	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 033 µF ±20%, 50 Vdc	930 313 016
C3	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 300 pF ±10%, 100 Vdc	930 164 307
CR1	DIODE:	943 113 511
M1 through M3	MICROCIRCUIT: F-02, Quad NAND gate integrated circuit	950 100 002
Q1	TRANSISTOR: Silicon, NPN	943 722 002
R1	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	932 007 049
R2	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4W	932 007 020

PARALLEL TRANSFER GATE PAC, MODEL CM-022

The Parallel Transfer Gate PAC, Model CM-022 (Figure CM-022-1), utilizes seven F-01 dual NAND gate microcircuits containing 14 2-input NAND gates without collector resistors. These circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The PAC can be used for the common transfer control of up to fourteen data signals. The data when transferred is inverted in polarity.

CIRCUIT FUNCTION

The NAND gates are arranged in four independent groups. Two of the groups contain four NAND gates each, one input being common to the four gates. The remaining two groups contain three NAND gates each, one input being common to the three gates.

Each gate performs the NAND function with conventional positive logic (+6V = ONE, 0V = ZERO). When both inputs are at passive or open, the output transistor is turned on, and the output is active (ground). If any input is at ground, the transistor is turned off, and the output is passive (the supply voltage, +6V).

The four common inputs can be externally connected to transfer a maximum of 14 bits of data simultaneously. With this arrangement, the data to be transferred is connected to the individual input of each gate and a strobe input is applied to the common input.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Input Loading

Individual inputs: 1 unit load each

Common inputs: 1 unit load per gate

Output Drive Capability

8 unit loads

Circuit Delay (measured at +1.5V averaged over two stages)

30 ns (max)

Current Requirements

+6V: 95 mA (max)

Power Dissipation

560 mW (max)

Electrical Parts List

Ref. Designation	Description	3C Part No.
M1-M7	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µF ±20%, 50 Vdc	930 313 016

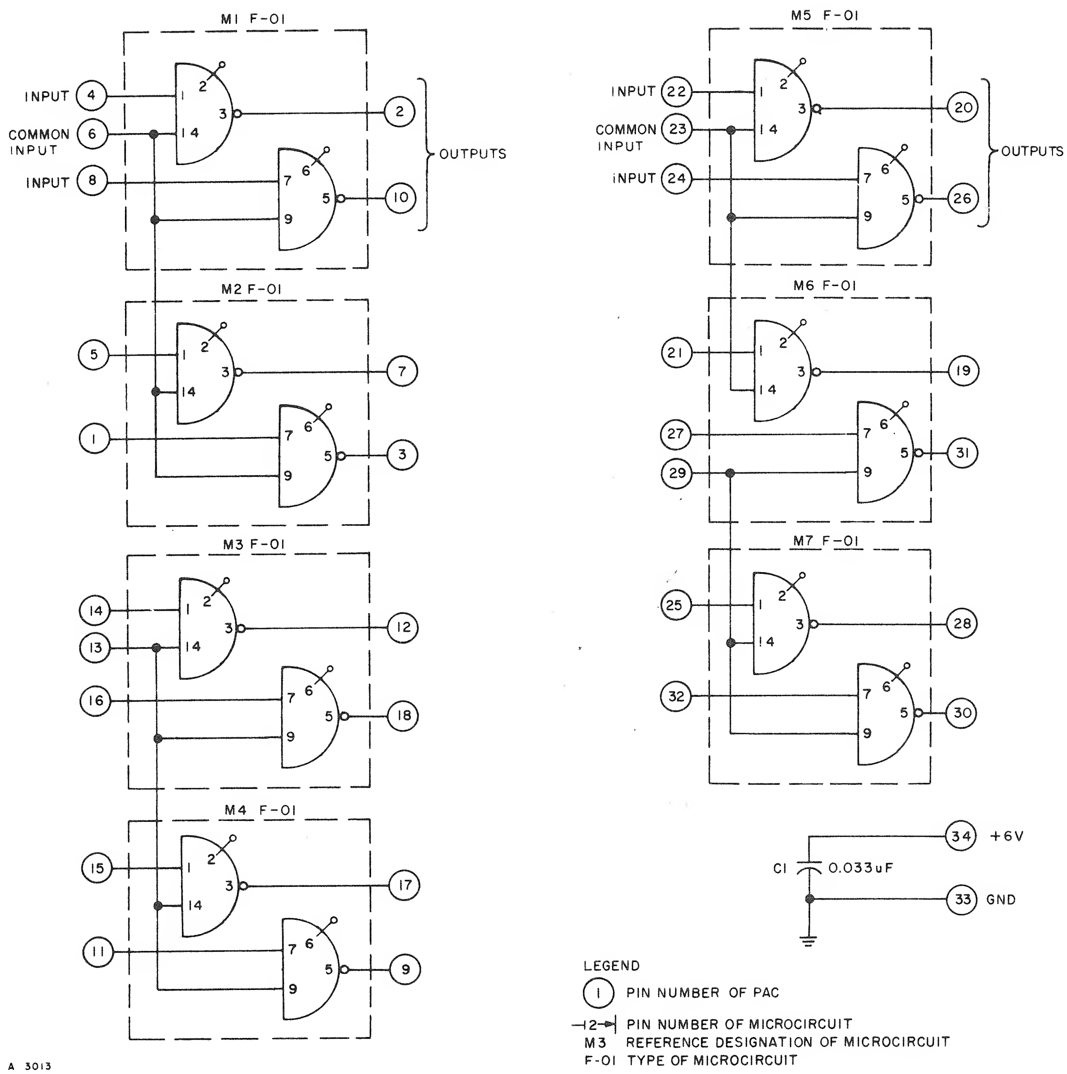


Figure CM-022-1 Parallel Transfer Gate PAC, Schematic Diagram

DELAY MULTIVIBRATOR PAC, MODEL NC-001

The model NC-001 μ-PAC is identical to the DM-335 u-PAC except as follows:-

C5:	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 4,700 pF ±2%, 50 Vdc	930 313 309
C12, C13	CAPACITOR, FIXED, .001 μF ±10%, 50 Vdc	930 164 309
Delay:-	Circuit A 20 micro-seconds	
	Circuit B 100 nano-seconds	

DELAY MULTIVIBRATOR PAC, MODEL NC-002

The model NC- 002 μ-PAC is identical to the DM-335 μ-PAC except as follows:-

C5, C10:	CAPACITOR, FIXED, TANTALUM: 3.3 μF ±2%, 75 Vdc	930 700 114
C12, C13:	CAPACITOR, FIXED, 001 μF ±10%, 50 Vdc	930 164 309
R3, R7:	RESISTOR, FIXED, FILM: 6.8K ±2%, 1/4W	932 114 069
Delay:-	Both circuits 15.3 milli-seconds	

DELAY MULTIVIBRATOR PAC, MODEL NC-003

The model NC-003 μ-PAC is identical to the DM-335 μ-PAC except as follows:-

C5:	CAPACITOR, FIXED, TANTALUM: 4.7 μF ±5%, 20 Vdc	930 235 006
C10:	CAPACITOR, FIXED, TANTALUM: 1.0 μF ±5%, 20 Vdc	930 235 042
C12, C13:	CAPACITOR, FIXED, .001 uF ±10%, 50Vdc	930 164 309
R7:	RESISTOR, FIXED, FILM: 5.1K ±2%, 1/4 W	932 114 066
Delay:-	Circuit A 8 milli-seconds	
	Circuit B 3.75 milli-seconds	

DELAY MULTIVIBRATOR PAC, MODEL NC-004

The model NC-004 μ-PAC is identical to the DM-335 μ-PAC except as follows:-

C5:	CAPACITOR, FIXED, TANTALUM: 2.2 μF ±5%, 10 Vdc	930 235 044
C12, C13:	CAPACITOR, FIXED, .001 μF ±10%, 50 Vdc	930 164 309
R3:	RESISTOR, FIXED, FILM: 5.1K ±2%, 1/4 W	932 114 066
Delay:	Circuit A 8 milli-seconds	
	Circuit B 1 micro-second	

MASTER CLOCK PAC, MODEL NC-005

The model NC-005 μ-PAC is identical to the MC-335 μ-PAC except as follows:-

Y1:	CRYSTAL UNIT, QUARTZ 284.2 KHz	961 002 204 *

MASTER CLOCK PAC, MODEL NC-006

The model NC-006 μ-PAC is identical to the MC-335 μ-PAC except as follows:-

Y1:	CRYSTAL UNIT, QUARTZ 204.2 KHz	961 002 204 *

* The crystal part number does not specify a particular frequency, but a range of frequencies and a physical size.

LBD No. EO33

4

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	TG-335	11	11	11	11	11	11	11	11	10	10	10	10	10	10
7	DL-335	27	10	10	11	10	11								
6	DI-335	11	11	11	11	11	11	11	11	11	11				
5	TG-335	10	10	10	10	10	13	10	10	10	10	10	10	10	10
4	OD-335	10	11	10											
3	DL-335	11	11	11	11	11	13								
2	TG-335	10	10	10	10	10	10	10	10	10	10	10	10	10	10
1	DI-335	10	10	10	10	13	13	11	11	11	11				

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CC-089	13	13	13	27										
7	CC-089	13	13	13	13										
6	TG-335	25	25	25	25	13	13	13	13	25	25	25	25	13	13
5	CC-092	13	13	25	26	25	13								
4	CC-088	25	25	25	11	25	25								
3	DL-335	25	25	25	25	25	25								
2	DI-335	25	25	22	13	13	26	26	13	25	13				
1	CC-138	13	13												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN		DEVICE D CABLE A												
7	DI-335	20	20	20	16	20	16	16	16	16	20				
6	DI-335	16	16	16	16	16	16	16	16	16	16				
5	CM-022	16	16	16	16	16	16	16	16	16	16	16	16	16	+
4	CM-022	16	16	16	16	16	16	16	16	16	16	16	16	16	+
3	CC-165	20	20	20	20	20	X								
2	CC-165	20	20	20	20	20	20								
1	CONN		DEVICE C CABLE B												

4 3

3

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	DL-335	13	26	26	26	25	13								
7	CC-092	31	26	13	26	26	26								
6	CC-088	31	31	31	31	31	31								
5	DI-335	22	22	22	22	22	22	22	27	27	27				
4	DI-335	31	31	31	31	27	27	27	27	23	24				
3	EO-335	31	31	31	31	31	27								
2	DN-335	22	24	23	25	22	23								
1	DG-335	22	22	22	31	31	22								

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CC-088	26	26	26	26	26	26								
7	NC-006	25	X												
6															
5	CC-089	27	27	27	27										
4	NC-005	25	X												
3															
2	CC-089	27	13	11	26										
1	NC-003	13	13												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN		DEVICE C CABLE A												
7	CC-165	20	20	20	20	20	20								
6	DI-335	19	19	19	15	19	15	15	15	15	19				
5	DI-335	15	15	15	15	15	15	15	15	15	15				
4	CM-022	15	15	15	15	15	15	15	15	15	15	15	15	15	+
3	CM-022	15	15	15	15	15	15	15	15	15	15	15	15	15	+
2	CC-165	19	19	19	19	19	X								
1	CONN		DEVICE B CABLE B												

3 2

2

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	DL-335	27	25	27	24	23	23								
7	DI-335	23	23	23	23	23	22	13	24	23	23				
6	TG-335	22	23	23	23	31	31	31	31	31	31	31	27	27	27
5	EO-335	23	23	23	31	31	31								
4	EO-335	23	23	23	23	23									
3	CC-088	24	24	24	24	24	31								
2	CC-092	22	22	22	22	22	22								
1	NC-001	24	13												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	PA-336	27	X	24	27	27	27								
7	DI-335	27	27	27	10	27	27	26	26	27	26				
6	TG-335	27	27	27	27	27	27	26	26	27	27	27	27	27	27
5	CC-092	29	29	29	29	29	29								
4	CM-022	30	30	30	30	30	30	30	30	30	30	+	30	30	+
3	CC-088	25	25	25	25	25	25								
2	TG-335	30	30	30	30	30	30	30	30	30	30		30	30	
1	NC-002	26	26												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN		DEVICE B CABLE A												
7	CC-165	19	19	19	19	19	19								
6	CC-165	19	19	19	19	19	19								
5	CC-130														
4	CC-092	18	18	18	19	19	15								
3	PA-336	14	14	14	15	15	15								
2	CC-165	18	18	18	18	18	X								
1	CONN		DEVICE A CABLE B												

2

1

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CC-092	24	24	24	24	24	24								
7	TG-335	22	22	22	22	22	22	22	22	13	24	24	24	24	24
6	CC-089	23	22	24	X										
5	DC-335	23	23	23	+	24	24								
4	DN-335	25	23	24	27	23	23								
3	CC-092	23	23	23	23	23	23								
2	TG-335	28	28	28	28	14	15	16	17	26	X	11	27	25	25
1	DM-335	27	24												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CC-092	29	29	29	29	29	29								
7	CC-092	29	29	29	29	29	29								
6	CC-152	29	29	29	29	29	29	29	29	29	29	29	29	29	29
5	FF-335	29	28	28	28	28	28	28	28						
4	TG-335	28	28	28	28	28	28	28	28	28	28	28	28	28	28
3	FF-335	28	28	28	28	28	28	28	28						
2	TG-335	28	28	28	28	28	28	28	28	28	28	28	28	28	28
1	CONN		I/O BUS												

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN		DEVICE A CABLE A												
7	CC-165	18	18	18	18	18	18								
6	CC-165	18	18	18	18	18	18								
5	DI-335	18	18	18	18	18	14	14	14	14	18				
4	DI-335	14	14	14	14	14	14	14	14	14	14				
3	TG-335	14	14	14	14	14	14	14	14	14	14	14	14	14	+
2	TG-335	14	14	14	14	14	14	14	14	14	14	14	14	14	+
1	CONN		I/O BUS												

A B C

NOTES
1. X SPARE
2. + TIED SPARE
3. NO GATE
4. 2 3 4 USED WITH 2nd, 3rd AND 4th MTT
5. 5 USED WITH DMC/DMA SUBCHANNEL
6. PACS VIEWED FROM WIRING SIDE
7. NUMBERS DENOTE ASSOCIATED LOGIC BLOCK DIAGRAM

REVISIONS REV CHK

Honeywell
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DR. DATE
ENG.
APP.
PROJECT No.

TITLE
PACKAGE COMPLEMENT
TAPE CONTROL UNIT
SERIES 16 4110

SIZE C DWG. No. D42503006 FROM SHT 1 OF 2 REV

A B C D E F G H J K L

LBD No. E034

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

1 2 3 4 5 6 7 8 9 10 11

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

5

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
8	CONN		RESERVED FOR DMC/DMA													
7	DI-335	12	12	12	12	24	13	23	25	13	14					
6	DI-335	12	12	12	12	12	12	12	12	12	12					5
5	DI-335	12	12	12	12	12	12	12	12	12	12					
4	DL-335	12	12	12	12	12	12									
3	CC-089	12	12	12	12											5
2	TG-335	10	10	10	10	11	11	11	11	11	11	11	11	11	11	
1	CC-151	11	11	11	11	11	11	11	11	29	29					

A

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
8	CONN		I/O BUS													
7	CC-139	13	13													
6	NC-004	26	25													
5	DI-335	13	11	10	10	27	13	12	12	⊠	⊠					
4	CC-165	21	21	21	21	21	⊠									4
3	CC-165	21	21	21	21	21	21									
2	CC-165	21	21	21	21	21	21									4
1	DM-335	25	13													

B

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
8	CONN		I/O BUS													
7	DI-335	21	21	21	17	21	17	17	17	17	21					4
6	DI-335	17	17	17	17	17	17	17	17	17	17					
5	CM-022	17	17	17	17	17	17	17	17	17	17	17	17	17		
4	CM-022	17	17	17	17	17	17	17	17	17	17	17	17	17		4
3	CC-092	20	20	16	21	21	17									
2	PA-336	16	16	16	17	17	17									
1	CONN		DEVICE D CABLE B													4

C

NOTES
1. ⊠ SPARE
2. ⊞ TIED SPARE
3. ⊟ NO GATE
4. △4 USED WITH 4th MTT
5. △5 USED WITH DMC/DMA SUBCHANNEL
6. PACS VIEWED FROM WIRING SIDE
7. NUMBERS DENOTE ASSOCIATED LOGIC BLOCK DIAGRAM

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SERIES 16 4110

SIZE	DWG. No.	FROM	REV
C	D42503006 SHT 2 OF 2		